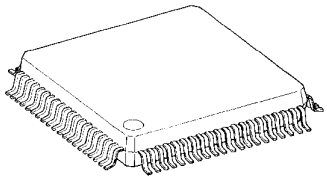
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9328AF

Portable Audio DTS Controller (DTS-21)

The TC9328AF is a single-chip DTS microcontroller for portable audio incorporating 230 MHz prescaller, PLL, and LCD driver. In addition to a 20-bit IF counter, 6-bit A/D converter, serial interface, and buzzer function, the device supports an interrupt function, 8-bit timer/counter, and 8-bit pulse counter. The LCD driver features built-in 1/4 duty, 1/2 bias and a 3 V voltage doubler boosting circuit, implementing stable LCD.

The power supply voltage ranges from 0.9 to 1.8 V. Because of its low-current consumption (CPU: 80 µA (max)), the device is suitable for use in digital tuning systems in portable equipment such as headphone stereos.



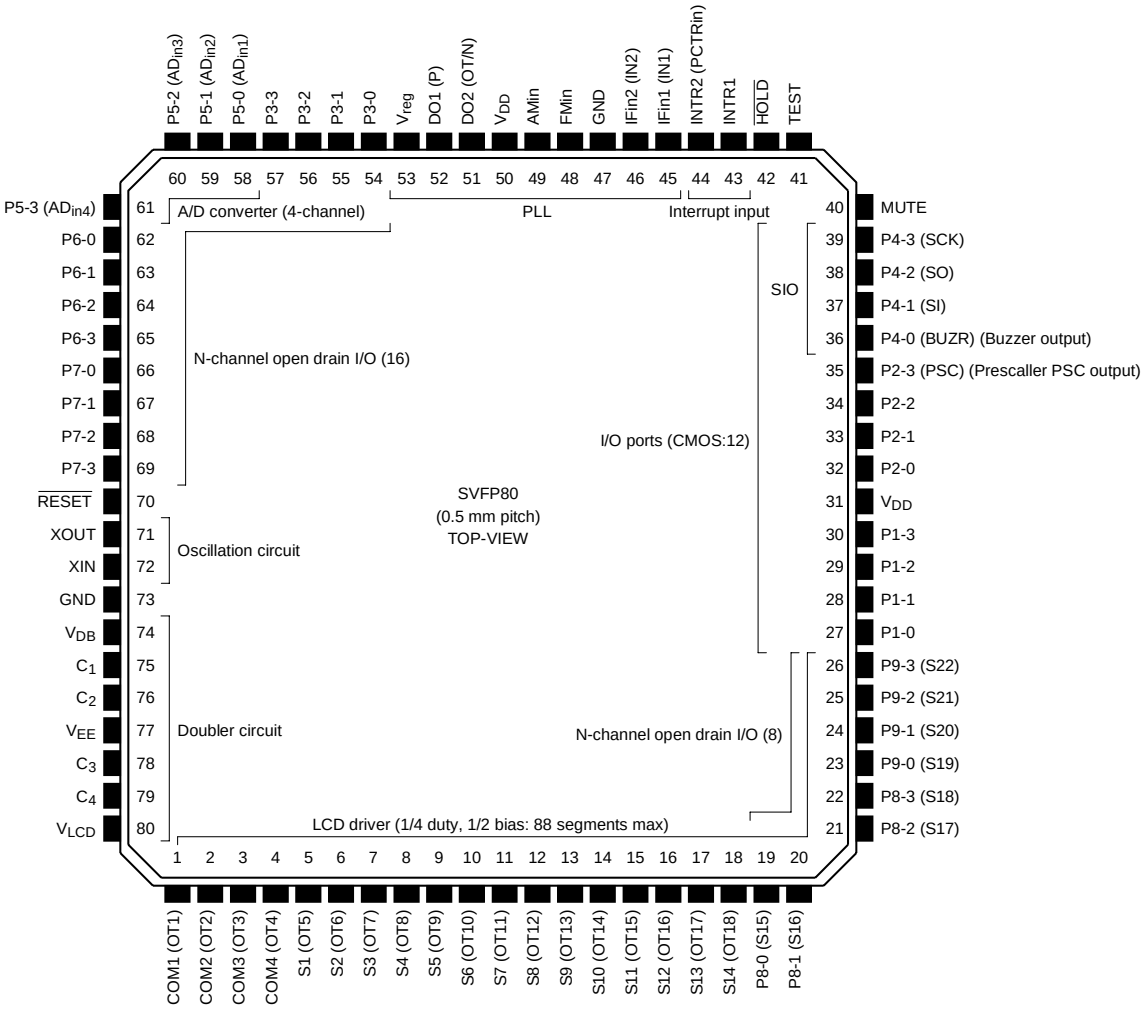
LQFP80-P-1212-0.50A

Weight: 0.45 g (typ.)

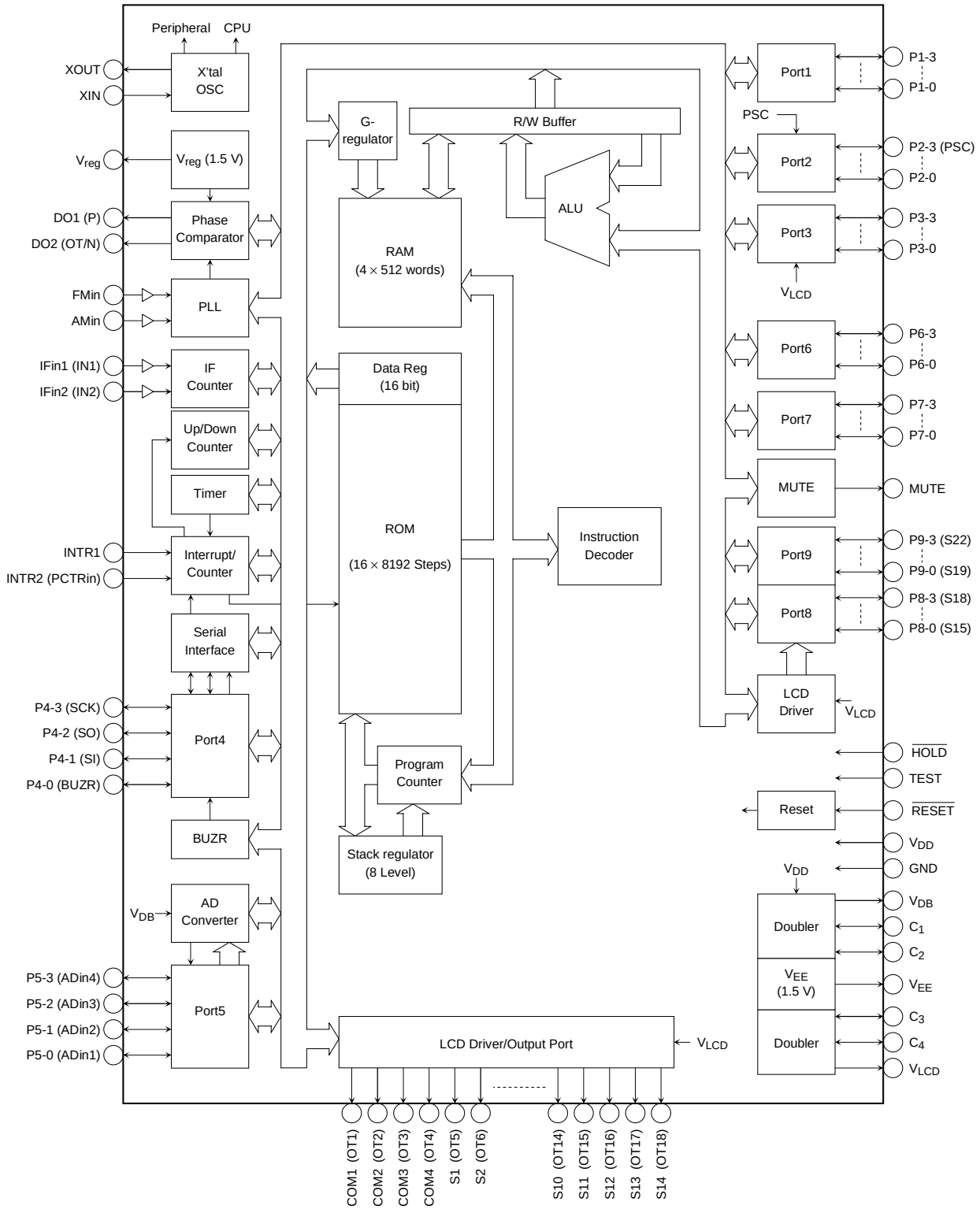
Features

- CMOS DTS microcontroller LSI with built-in 230 MHz prescaller, PLL, and LCD driver
- Operating voltage: V_{DD} = 0.9 to 1.8 V (typ.: 1.5 V)
- Current dissipation:
  When CPU in operation: I_{DD} = 40 µA (typ.)
  When PLL in operation: I_{DD} = 6 mA (typ.) (VHF mode)
- Operating temperature range: Ta = −10 to 60°C
- Program memory (ROM): 16-bit × 8192 steps
- Data memory (RAM): 4-bit × 512 words
- Instruction execution time: 40 µs
- Crystal oscillator frequency: 75 kHz
- Stack level: 8
- General-purpose IF counter: 20-bit (CMOS input supported)
- A/D converter: 6-bit × 4 channel
- LCD driver: 1/4 duty, 1/2 bias, 88 segments (max)
- I/O port: CMOS I/O ports: 12
  N-channel open drain I/O ports: 24 (max)
  Output-only port: 1
  Input-only ports: 5 (max)
- Timer/counter: 8-bit (as timer clock: INTR1/INTR2, instruction cycle: 1 kHz selectable)
- Pulse counter: 8-bit up/down counter (input via INTR2 pin)
- Buzzer: Built-in four mode: 0.625 to 3 kHz (8 types), Continuous, Single-Shot, 10 Hz Intermittent, or 10 Hz Intermittent 1 Hz Interval
- Package: QFP-80 (0.5 mm pitch, 1.4 mm thick)

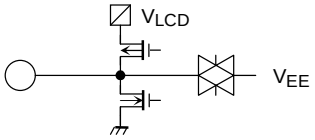
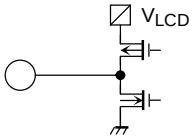
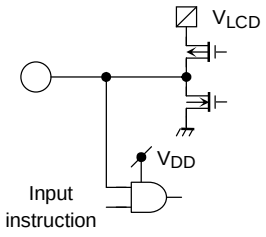
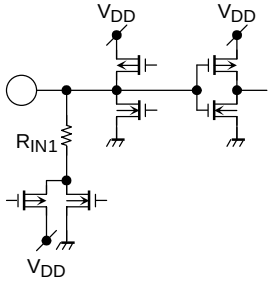
Pin Assignment



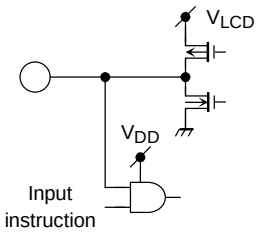
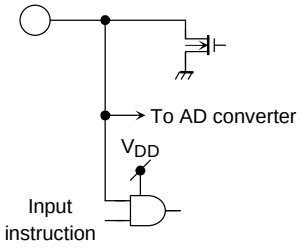
Block Diagram

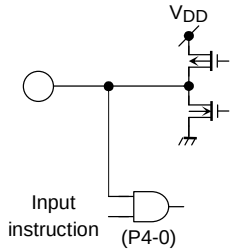
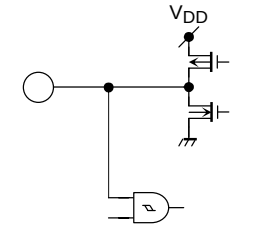
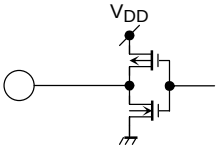
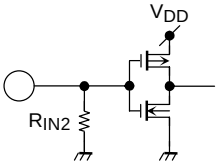


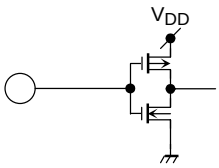
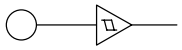
Description of Pin Function

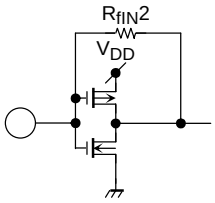
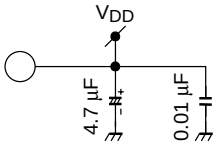
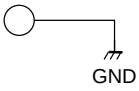
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
1	COM1/OT1	LCD common output/Output port	Output common signals to LCD panels. Through a matrix with pins S1 to S22, a maximum 88 segments can be displayed. Three levels, V_{LCD}, V_{EE}, and GND, are output at 62.5 Hz every 2 ms. V_{EE} is output after system reset and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0". These pins can be programmed as output ports (Note 1).	
2	COM2/OT2			
3	COM3/OT3			
4	COM4/OT4			
5~18	S1/OT5~ S14/OT18	LCD segment output/Output port	Segment signal output pins for LCD panel. Together with COM1 to COM4, a matrix is formed that can display a maximum of 88 segments. All pins from S1 to S14 can be programmed as output ports (Note), and all pins from S15 to S22 as I/O ports, in units of pins. When the pins function as output ports, V_{LCD} pin potential and GND potential are output to them. When the pins function as I/O ports, drain output is N-ch open. Because power is supplied from V_{LCD} for the I/O ports, up to V_{LCD} voltage (3 V) can be applied. These data ports (OT1 to OT18) are incremented by 1 by instruction every time data are accessed. Therefore, they can be used for external memory address signals, facilitating data access. Note: After system reset, the output port pins are set to LCD output, the I/O port pins to I/O port input.	
19~26	P8-0/S15~ P9-3/S22	LCD segment output/ I/O port		
27~30	P1-0~P1-3	I/O port 1	The input and output of these 4-bit I/O ports can be programmed in 1-bit units. These pins can be programmed to be pulled up or down. Thus, they can be used as key input pins. By altering the input of I/O ports set to input, the CLOCK STOP mode or the WAIT mode can be released, and the MUTE bit of the MUTE pin can be set to "1".	

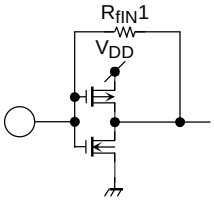
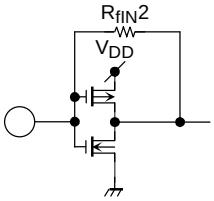
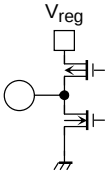
Note 1: When the LCD pin is set as an output port, the "H" level output is the doubled voltage V_{LCD}. Therefore, disconnect the voltage doubler boosting capacitor but connect the V_{LCD} pin to the V_{DD} pin.

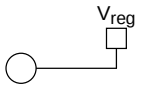
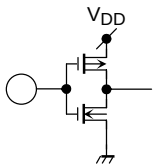
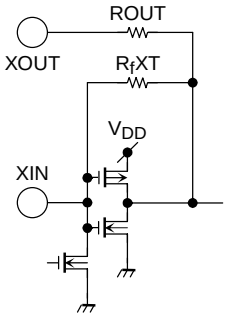
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
32~34	P2-0~P2-2	I/O port 2	The input and output of these 4-bit I/O ports can be programmed in 1-bit units. The P2-3 pin is also used as a PLL prescaller PSC signal output pin. A PLL can be configured using an external prescaller. In such a case, set the pin to I/O port output.	
35	P2-3/PSC	I/O port 2 /Prescaller /PSC output		
54~57	P3-0~P3-3	I/O port 3	4-bit I/O ports, allowing input and output to be programmed in 1 bit units. Pins P5-0 to P5-3 can also be used for analog input to the built-in 6-bit, 4-channel AD converter. The conversion time of the built-in AD converter using the successive comparison method is 280 μs. The necessary pin can be programmed to AD analog input in 1-bit units. Up to the doubled voltage V_{DB} ($V_{DD} \times 2$) can be input as the AD input voltage. The I/O ports are N-ch open drain output. Up to the V_{DB} voltage can be applied to the AD input pins, and up to 3.6 V can be applied to the I/O port pins. I/O port 3 can obtain N-ch high-output current (2 mA typ.) even at low voltage. The AD converter and all associated controls are performed via sortware.	
58~61	P5-0/AD_{in1}~ P5-3/AD_{in4}	I/O port 5 /AD analog voltage input		
62~69	P6-0~P7-3	I/O port 6, 7		

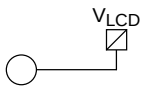
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
36~39	P4-0/BUZR P4-1/SI P4-2/SO P4-3/SCK	I/O port 4 /Buzzer output /Serial data input /Serial data output /Serial clock I/O	4-bit I/O ports, allowing input and output to be programmed in 1-bit units. The P4-0 pin is also used for buzzer output. P4-1 to P4-3 are also used as serial interface circuit (SIO) input / output pins. The buzzer output can select 8 kinds of 0.625 to 3 kHz frequencies with 4 modes: continuous output, single-shot output, 10 Hz intermittent output, and 10 Hz intermittent 1 Hz interval output. SIO functions for 4-bit or 8-bit serial data inputs from the SI pin and outputs from the SO pin at the SCK pin clock edge. The clock for serial operation (SCK) is capable of internal (SCK = 37.5 kHz)/ external options and rise/fall shift options. The SO pin is also capable of switching to serial inputs (SI), facilitating the control of various LSI's and communication between controllers. When SIO interrupts are enabled, an interrupt is generated after SIO execution and the program jumps to address 4. This is useful for high-speed serial communications. All SIO inputs use built-in Schmitt circuits. P3-3 pins also functions as the output for a built-in buzzer. SIO, buzzer, and all associated controls can be programmed.	  Input instruction + SIOon (P4-1~P4-3)
40	MUTE	Muting output port	1-bit output port, normally used for muting control signal output. This pin can set the internal MUTE bit to "1" according to a change in the input of I/O port 1 and $\overline{\text{HOLD}}$. MUTE bit output logic can be changed.	
41	TEST	Test mode control input	Input pin used for controlling TEST mode. "H" (high) level indicates TEST mode, while "L" (low) indicates normal operation. The pin is normally used at low level or in NC (no connection) state. (A pull-down resistor is builtin).	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
42	$\overline{\text{HOLD}}$	Hold mode control input	Input pin for request/release hold mode. Normally, this pin is used to input radio mode selection signals or battery detection signals. Hold mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. To request Clock Stop mode, either L-level detection on the $\overline{\text{HOLD}}$ pin or forced execution can be programmed. The mode is released by H-level detection on the $\overline{\text{HOLD}}$ pin or input change, respectively. Executing the CKSTP instruction stops the clock generator and the CPU, entering memory backup state. In memory backup state, current dissipation becomes low (1 μA or less) and the display output/CMOS output ports automatically become L level and N-ch open drain output Off. Regardless of this input state, Wait mode is executed in order to lower power dissipation. Either crystal oscillator only in operation or CPU suspension can be programmed. For crystal oscillator only in operation, all displays are at L level and other pins are in hold state. For CPU suspension, the CPU stops and all others retain their states. Wait mode is released by changing $\overline{\text{HOLD}}$ input.	
43 44	INTR1 INTR2 /PCTRin	External interrupt input /Pulse counter input	External interrupt input pins. When interrupts are enabled and a 13.3 to 26.7 ms pulse or longer is input to the pin, interrupt INTR1/2 is generated and the program jumps to address 1/2. Input logic or rising/falling edge can be selected for each input interrupt. The internal 8-bit timer clock input can be selected as input to the pins. When the count value reaches the specified value, an interrupt is generated (address 3). The pin is also used for input of an 8-bit pulse counter. Input rising/falling or upcount/downcount can be selected for the counter. These inputs use built-in Schmitt circuits. The pins can also be used as input ports for input of remote control signals or a tape count.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
45 46	IFin1/IN1 IFin2/IN2	IF signal input /Input port	IF signal input pin for the IF counter to count the IF signals of the FM and AM bands and to detect the automatic stop position. The input frequency is between 0.3 to 12 MHz. A built-in input amp. and C coupling allow operation at low-level input. The IF counter is a 20-bit counter with optional gate times of 1, 4, 16 and 64 ms. 20 bits of data can be readily stored in memory. In Manual mode, gate On/Off can be performed using instruction. The input pin can be programmed for use as an input port (IN port). Note: When a pin is set to IF input, the input is at high impedance in PLL Off mode or if the pins are not used for input.	
31, 50	V_{DD}	Power-supply pins	Pins to which power is applied. Normally, V_{DD} = 0.9~1.8 V is applied. For the PLL, power for the prescaller in the programmable counter block and IF input amp can be individually programmed. By switching to different modes depending on the power supply voltage and the frequency used, current dissipation can be lowered. Connect a stabilizing capacitor between the V_{DD} pin and GND (4.7 μF, 0.01 μF typ.). In backup state (at execution of the CKSTP instruction), current dissipation drops (1 μA or less) and the power supply voltage can be reduced to 0.75 V. If more than 0.9 V is applied when the pin voltage is 0, the device system is reset and the program starts from address “0”. (Power on reset) Note: To operate the power on reset, the power supply should start up in 10~100 ms. Note: The power-on reset function can be enabled/disabled using the AI switch.	
47, 73	GND			

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
48	FMin	FM local oscillation signal input	Programmable counter input pin for FM/AM band. For FM input, mode can be switched between 1/2 + Pulse Swallow VHF and FM mode. For AM input, mode can be switched between Pulse Swallow (HF) and Direct Dividing (LF) mode. Normally, local oscillation output (Voltage-Controlled Oscillator: VCO output) of 50 to 230 MHz is input in VHF mode; 30 to 130 MHz in FM mode; 1 to 30 MHz in HF mode; 0.5 to 8 MHz in LF mode.	
49	AMin	AM local oscillation signal input	A PLL can be configured using an external prescaller. In such a case, set the pin to LF, and connect the prescaller divider output to the AMin input pin and the PSC input to the P2-3 (PSC) output pin. With an input amp incorporated, capacitive-coupling, small-amplitude operation. Note: The input is at high impedance in PLL Off mode or if the pins are not used for input.	
52 51	DO1/P DO2/OT/N	Phase comparator output/output port /P output Phase comparator output/output port /N output	PLL phase comparator output pins. Tristate output. When the program counter divider output is higher than the reference frequency, H level is output; when lower, L level; and when they match, high impedance. For the phase comparator power supply, a 1.5 V constant voltage supply (V_{reg} pin) is used. Even if the power supply voltage drops, a stable PLL can be configured. Because DO1 and DO2 are output in parallel, a filter constant can be optimally designed for each FM/AM band. The DO2 pin can be programmed to high impedance or as an output port (OT). Therefore, using the DO1 and DO2 pins, lockup time can be improved or the pins can be effectively used as output ports. Also, the phase comparator charge pump control signal (P/N) can be output from the DO1/2 pin by program so a PLL using an external charge pump can be configured. In such a case, when the program counter divider output is higher than the reference frequency, P/N is output at H/L level; when lower, L/H level; and when they match, L/L level. When set to this mode, H level output becomes V_{DD} level. Note: For tristate output, the H level output uses a constant voltage supply. When H level output current is required, Toshiba recommend using an external power supply.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
53	V_{reg}	Phase comparator constant voltage supply	Phase comparator constant voltage supply. When the phase comparator output is tristate output, a constant voltage supply of 1.5 V (typ.) is output to the pin. For this output, connect a stabilizing capacitor (0.47 μF typ.). At constant voltage operation, the H level phase comparator output uses a constant voltage. Thus, when H level output current is required, Toshiba recommend using an external power supply. In such a case, externally apply 1.8~3.6 V to the pin. When the phase comparator output is output using the charge pump control signal (P/N), the pin becomes the V_{DD} level. Then, the phase comparator output operates using the power supply voltage.	
70	$\overline{\text{RESET}}$	Reset input	Input pin for system reset signals. $\overline{\text{RESET}}$ takes place while at low level; at high level, the program starts from address “0”. Normally, if more than 0.9 V is supplied to V_{DD} when the voltage is 0, the system is reset (power on reset). Accordingly, this pin should be set to high level during operation. Note: When the power-on reset function is enabled/disabled using the AI switch, reset by pin.	
71	XOUT	Crystal oscillator pin	Crystal oscillator pins. A reference 75 kHz crystal oscillator is connected to the XIN and XOUT pins. The oscillator stops oscillating during CKSTP instruction execution. The VXT pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.47 μF typ.) is connected.	
72	XIN			

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
74	V_{DB}	Voltage doubler boosting output pins	Voltage doubler boosting output pins. The V_{DB} pin doubles the V_{DD} pin voltage using the voltage doubler boosting capacitor between C_1 and C_2. The doubled voltage is used for the AD converter and constant voltage circuit (V_{reg}, V_{EE}) power supply. The V_{EE} pin supplies a constant voltage of 1.5 V from the V_{DB} voltage. The voltage is doubled (to 3 V) using the voltage doubler boosting capacitor between C_3 and C_4. The doubled voltage is then supplied to the V_{LCD} pin. The V_{EE} potential and the V_{LCD} potential are used to drive the LCD. Connect a stabilizing capacitor between the V_{DB} pin and GND (0.1 μF, 10 μF typ.), and between the V_{LCD} pin and GND (0.1 μF typ.). Connect a voltage doubler boosting capacitor (0.1 μF typ.) between C_1 and C_2, and between C_3 and C_4. (Note 1)	
75	C_1			
76	C_2			
77	V_{EE}			
78	C_3			
79	C_4			
80	V_{LCD}			

Note 1: When the LCD pin is set as an output port, the “H” level output is the doubled voltage V_{LCD}. Therefore, disconnect the voltage doubler boosting capacitor but connect the V_{LCD} pin to the V_{DD} pin.

Description of Operations

○ CPU

The CPU consists of a program counter, a stack register, ALU, a program memory, a data memory, G-register, a data register, DAL address register, carry F/F, a judgment circuit, and an interruption circuit.

1. Program Counter (PC)

The program counter consists of a 14-bit binary up-counter and addresses the program memory (ROM). The counter is cleared when the system is reset and the programs start from the 0 address.

Under normal conditions, the counter is increased in increments of one whenever an instruction is executed, but the address specified in the instruction operand is loaded when a JUMP instruction or CALL instruction is executed.

Also, when an instruction that is equipped with the skip function (AIS, SLTI, TMT, RNS instructions, etc.) is executed and result of this includes a skip condition, the program counter is increased in increments of two and the subsequent instruction is skipped. Furthermore, if interruption is received, the vector address corresponding to each interruption is loaded.

Note: Program memory (ROM) It is 0000H-0FFFH address.
For this reason, an access setup to the address beyond this is forbidden.

Instruction	Contents of Program Counter (PC)													
	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
JUMP ADDR1	← Operand of instruction (ADDR1) →													
JUMP ADDR2	0	0	← Operand of instruction (ADDR2) →											
Power on reset RESET by reset pin	0	0	0	0	← Operand of instruction (ADDR3) →						← Contents of general register (r) →			
DAL (DA) (DAL bit = 1)	← DAL address register (DA) →													
RN, RNS, RNI	← Contents of stack register →													
At the time of an interruption reception	← Vector address of each interruption →													
Power on reset RESET by reset pin	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Priority	Interruption Factor	Vector Address
1	INTR1 pin	0001H
2	INTR2 pin	0002H
3	Serial inter face	0003H
4	Timer counter	0004H

2. Stack Register

A register consisting of 8 × 14 bits which stores the contents of the program counter +1 (the return address) when a sub-routine call instruction is executed, or an interrupt is processed. The contents of the stack register are loaded into the program counter when the return instruction (RN, RNS, RNI instruction) is executed.

There are eight stack levels available and nesting occurs up to eight levels.

3. ALU

ALU is equipped with binary 4-bit parallel add/subtract functions, logical operation, comparison and multiple bit judgment functions. This CPU is not equipped with an accumulator, and all operations are handled directly within the data memory.

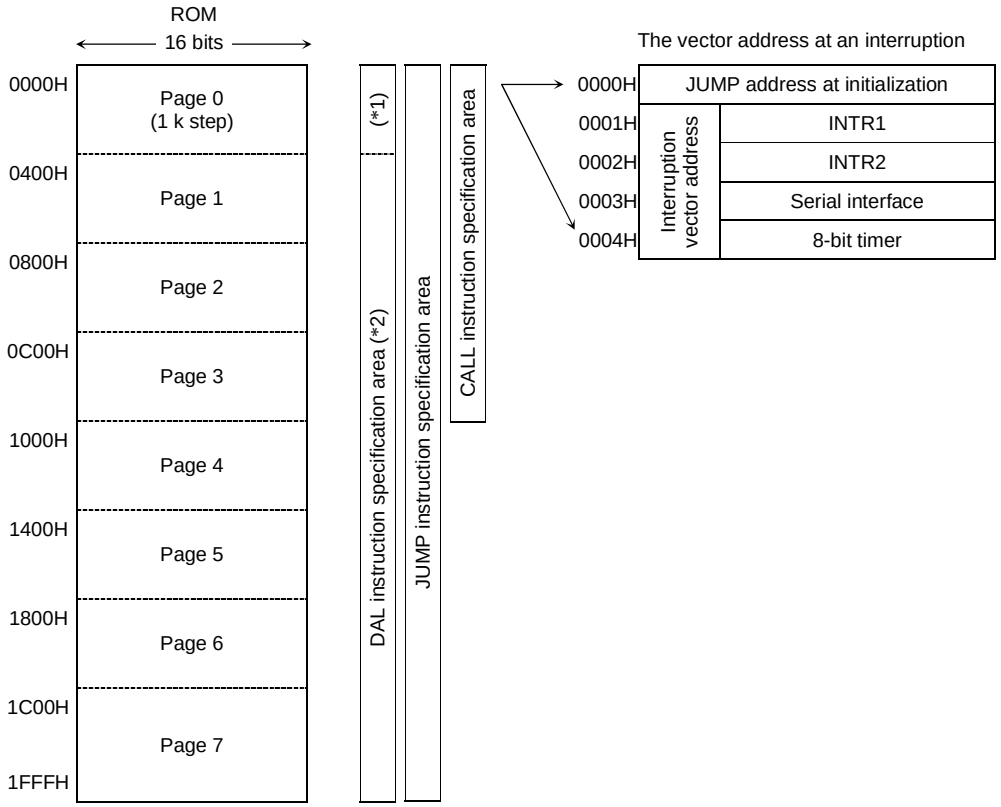
4. Program Memory (ROM)

The program memory consists of 16 bits × 16384 steps and is used for storing programs. The usable address range consists of 16384 steps between address 0000H and 1FFFH.

The program memory divids 16384 into 8 separate steps and consists of page 0 to 7. The JUMP instruction can be freely used throughout all 16384 steps though the Call instruction can use the address from 0000H to 0fffH from page 0 to 3.

In case of setting DAL bit, arranged on I/O map, "0" (DAL ADDR3, (r) command), the program memory address 0000H to 03FFH, page 0, are used as data area and setting DAL bit "1" (DAL (DA) command), the program memory address 0000H to 0FFFH (page 0 to 3) are used as data area. The 16-bit content of this can be loaded into the data register by executing the DAL instruction.

Note: Set the address for data area of program memory outside of the program loop.



*1: DAL bit = DAL access area at setting "0"

*2: DAL bit = DAL access area at setting "1"

Note: DAL bit is arranged on I/O map.

5. Data Memory (RAM)

The data memory consists of 4 bits × 512 words and used for storing data. These 512 words are expressed in row address (6 bits) and column addresses (4 bits). 348 words (row address = address 04H to 1FH) within the data memory are addressed indirectly by the G-register. Therefore, it is necessary to specify the row address with the G-register before the data in this area is processed.

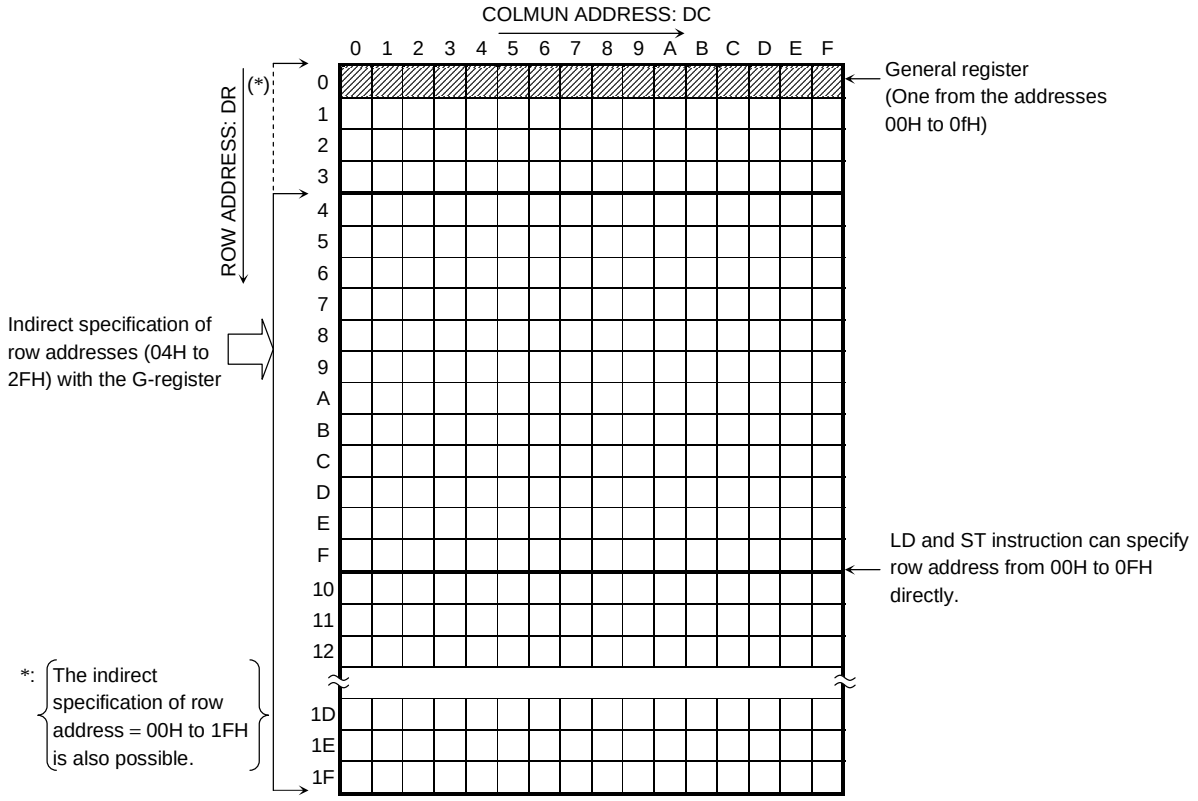
The address 00H to 0FH within the data memory are known as general registers, and these can be used simply by specifying the relevant column address (4 bits). These sixteen general registers can be used for operations and transfers with the data memory, and may also be used as normal data memories.

Note: The column address (4 bits) that specifies the general register is the register number of the general register.

Note: All row address (addresses 00H to 1FH) can be specified indirectly with the G-register.

Note: The data memory has 512 words and the highest bit of 6 in the G-register row address must be used “0” (00H - 1FH address).

Note: By using LD and ST instruction, it can be addressed directly in 256 words (row address = 00H to 0FH) in the data memory.



6. G-Register (G-REG)

The G-register is a 6-bit register used for addressing the row addresses (D_R = 04H to 2FH addresses) of the data memory's 448 words.

The contents of this register are validated when the MVGD instruction or MVGS instruction are executed, and not affected through the execution of any other instructions. This register is used as one of the ports, and the contents are set when the OUT1 instruction from among the I/O instructions is executed. The 6-bit contents can be directly set by execution of STIG instruction.
(→ Refer to the section in Register Ports.)

7. Data Register (DATA REG)

The data register consists of 1 × 16 bits and loads 16 bits of optional address data in the program memory at the DAL instruction executed. This register is used as one of the ports, and the contents are loaded into the data memory in units of 4 bits when IN1 instruction among the I/O instruction is executed. (→ Refer to the section in Register Ports.)

This register can be written from the data memory, and is used for the evacuation and the return processing of the data at the interruption.

8. DAL Address Register (DA)

The data register consists of 1 × 14 bits.

If DAL instruction is executed when the DAL bit is set to "1", 16 bits of the data of the free addresses in the program memory specified by this DAL address register are loaded. By the setting (DATA) → DA bit to "1", the contents of data register (DATA REG) can be transmitted to DAL address register (DA).

This register and a control bit are treated as a port, and are accessed by IN3/OUT3 instruction of an input-and-output instruction. (→ Refer to the register port item)

9. Carry F/F (Ca Flag)

This is set when either Carry or Borrow are issued in the result of calculation instruction execution and is reset if neither of these are issued.

The contents of carry F/F can only be amended through the execution of addition and, subtraction or, CLT and, CLTC instructions, and not affected by the execution of any other instruction.

The carry F/F can be accessed by IN1/OUT1 instruction of an input-and-output instruction. For this reason, the evacuation and the return at the time of interruption are performed by the input-and-output instruction between data memories. (Refer to the register port item)

10. Judgment Circuit (J)

This circuit judges the skip conditions when an instruction with the skip function is executed. The program counter is increased by two when the skip conditions are satisfied, and the subsequent instruction is skipped.

There are 15 instructions equipped with a wide variety of skip functions. (→ Refer to the items marked with a "*" symbol in the Table Instruction Functions and Operational Instructions)

11. Interruption Circuit

An interruption circuit branches into each vector address by the demand from peripheral hardware, and processes each interruption. (→ Refer to the interruption functional item)

12. Instruction Set Table

A total of 57 instruction sets is available, and all of these are single-word instructions.
These instructions are expressed with 6-bit instruction codes.

Upper 2 bits / Lower 4 bits		00		01		10	11	
		0		1		2	3	
0000	0	AI	M, I	TMTR	r, M		SLTI	M, I
0001	1	AIC	M, I	TMFR	r, M		SGEI	M, I
0010	2	SI	M, I	SEQ	r, M		SEQI	M, I
0011	3	SIB	M, I	SNE	r, M		SNEI	M, I
0100	4	ORIM	M, I	LD	r, M*	JUMP ADDR1	TMTN	M, N
0101	5	ANIM	M, I				TMT	M, N
0110	6	XORIM	M, I				TMFN	M, N
0111	7	MVIM	M, I				TMF	M, N
1000	8	AD	r, M	ST	M*, r		IN1	M, C
1001	9	AC	r, M				IN2	M, C
1010	A	SU	r, M				IN3	M, C
1011	B	SB	r, M				OUT1	M, C
1100	C	ORR	r, M	CLT	r, M	CAL ADDR2	OUT2	M, C
1101	D	ANDR	r, M	CLTC	r, M		OUT3	M, C
1110	E	XORR	r, M	MVGD	r, M		DAL	ADDR3, r
1111	F	MVSR	M1, M2	MVGS	M, r		SHRC	M
							RORC	M
							STIG	I*
							SKP, SKPN	
							RN, RNS	
							WAIT	P
							CKSTP	
							XCH	M
							DI, EI, RNI	
							NOOP	

13. Table of Instruction Functions and Operational Instructions

(Description of the symbols used in the table)

M	; Data memory address. Normally one of the addresses among the addresses 000H to 03FH in the data memory.
M*	; Data memory address (256 words) One of the addresses among the addresses 000H to 0FFH in the data memory. (Effective only when ST and LD instruction are executed.)
r	; General register One of the addresses among the addresses 000H to 00FH in the data memory.
PC	; Program Counter (14 bits)
STACK	; Stack register (14 bits)
G	; G-register (6 bits)
DATA	; Data register (16 bits)
I	; Immediate data (4 bits)
I*	; Immediate data (6 bits, effective only when STIG instruction is executed.)
N	; Bit position (4 bits)
—	; ALL "0"
C	; Port code No. (4 bits)
CN	; Port code No. (4 bits)
RN	; General register No. (4 bits)
ADDR1	; Program memory address (14 bits)
ADDR2	; Program memory address in the pages from 0 to 3 (12 bits)
ADDR3	; The upper 6 bits of the program memory address in the page 0.
DA	; DAL address register (14bits, effective only when DAL instruction, DAL bit = 1, is executed.)
Ca	; Carry
CY	; Carry flag
P	; Wait condition
b	; Borrow
IN1~IN3	; The ports used during the execution of instructions from IN1 to IN3
OUT1~OUT3	; The ports used during the execution of instructions from OUT1 to OUT3
( )	; Contents of the register or data memory
[ ] C	; Contents of the port indicated by the code No. C (4 bits)
[ ]	; Contents of the data memory indicated by the contents of the register or data memory
[ ] P	; Contents of the program memory (16 bits)
IC	; Instruction code (6 bits)
*	; Commands equipped with the skip function
DC	; Data memory column address (4 bits)
DR	; Data memory row address (2 bits)
DR*	; Data memory row address (4 bits, effective only when ST and LD instruction is executed)
(M) b0~(M) b3	; Bit data of the contents of a data memory (1 bit)

Instruc-tion Group	Mnemonic	Skip Function	Function Description	Operation Description	Machine Language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Addition Instructions	AI M, I		Add immediate data to memory	M ← (M) + I	000000	DR	DC	I
	AIC M, I		Add immediate data to memory with carry	M ← (M) + I + ca	000001	DR	DC	I
	AD r, M		Add memory to general register	r ← (r) + (M)	001000	DR	DC	RN
	AC r, M		Add memory to general register with carry	r ← (r) + (M) + ca	001001	DR	DC	RN
Subtraction Instructions	SI M, I		Subtract immediate data from memory	M ← (M) – I	000010	DR	DC	I
	SIB M, I		Subtract immediate data from memory with borrow	M ← (M) – I – b	000011	DR	DC	I
	SU r, M		Subtract memory from general register	r ← (r) – (M)	001010	DR	DC	RN
	SB r, M		Subtract memory from general register with borrow	r ← (r) – (M) – b	001011	DR	DC	RN
Comparison Instructions	SLTI M, I	*	Skip if memory is less than immediate data	Skip if (M) < I	110000	DR	DC	I
	SGEI M, I	*	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧ I	110001	DR	DC	I
	SEQI M, I	*	Skip if memory is equal to immediate data	Skip if (M) = I	110010	DR	DC	I
	SNEI M, I	*	Skip if memory is not equal to immediate data	Skip if (M) ≠ I	110011	DR	DC	I
	SEQ r, M	*	Skip if general register is equal to memory	Skip if (r) = (M)	010010	DR	DC	RN
	SNE r, M	*	Skip if general register is not equal to memory	Skip if (r) ≠ (M)	010011	DR	DC	RN
	CLT r, M		Set carry flag if general register is less than memory, or reset if not	(CY) ← 1 if (r) < (M) or (CY) ← 0 if (r) ≧ (M)	011100	DR	DC	RN
	CLTC r, M		Set carry flag if general register is less than memory with carry or reset if not	(CY) ← 1 if (r) < (M) + (ca) or (CY) ← 0 if (r) ≧ (M) + (Ca)	011101	DR	DC	RN

Instruction Group	Mnemonic	Skip Function	Function Description	Operation Description	Machine Language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Transfer Instructions	LD r, M*		Load memory to general register	r ← (M*)	0101	DR* (4 bits)	DC	RN
	ST M*, r		Store memory to general register	M* ← (r)	0110	DR* (4 bits)	DC	RN
	MVSR M1, M2		Move memory to memory in same row	(DR, DC1) ← (DR, DC2)	001111	DR	DC1	DC2
	MVIM M, I		Move immediate data to memory	M ← I	000111	DR	DC	I
	MVGD r, M		Move memory to destination memory referring to G-register and general register	[(G), (r)] ← (M)	011110	DR	DC	RN
	MVGS M, r		Move source memory referring to G-register and general register to memory (Note)	(M) ← [(G), (r)]	011111	DR	DC	RN
	STIG I*		Move immediate data to G-register	G ← I*	111111	I*		0010
I/O Instructions	IN1 M, C		Input IN1 port data to memory	M ← [IN1] C	111000	DR	DC	CN
	OUT1 M, C		Output contents of memory to OUT1 port	[OUT1] C ← (M)	111011	DR	DC	CN
	IN2 M, C		Input IN2 port data to memory	M ← [IN2] C	111001	DR	DC	CN
	OUT2 M, C		Output contents of memory to OUT2 port	[OUT2] C ← (M)	111100	DR	DC	CN
	IN3 M, C		Input IN3 port data to memory	M ← [IN3] C	111010	DR	DC	CN
	OUT3 M, C		Output contents of memory to OUT3 port	[OUT3] C ← (M)	111101	DR	DC	CN
Logical Instructions	ORR r, M		Logical OR of general register and memory	r ← (r) ∨ (M)	001100	DR	DC	RN
	ANDR r, M		Logical AND of general register and memory	r ← (r) ∧ (M)	001101	DR	DC	RN
	ORIM M, I		Logical OR of memory and immediate data	M ← (M) ∨ I	000100	DR	DC	I
	ANIM M, I		Logical AND of memory and immediate data	M ← (M) ∧ I	000101	DR	DC	I
	XORIM M, I		Logical exclusive OR of memory and immediate data	M ← (M) ∀ I	000110	DR	DC	I
	XORR r, M		Logical exclusive OR of general register and memory	r ← (r) ∀ (M)	001110	DR	DC	RN

Note: The execution period for the MVGS instruction is two machine cycles.

Instruction Group	Mnemonic	Skip Function	Function Description	Operation Description	Machine Language (16 bits) IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Bit Judgment Instruction	TMTR r, M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all "1"	010000	DR	DC	RN
	TMFR r, M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all "0"	010001	DR	DC	RN
	TMT M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all "1"	110101	DR	DC	N
	TMF M, N	*	Test memory bits, then skip if all bits specified are false	Skip if M (N) = all "0"	110111	DR	DC	N
	TMTN M, N	*	Test memory bits, then not skip if all bits specified are true	Skip if M (N) = not all "1"	110100	DR	DC	N
	TMFN M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = not all "0"	110110	DR	DC	N
	SKP	*	Skip if carry flag is true	Skip if (CY) = 1	111111	00	—	0011
	SKPN	*	Skip if carry flag is false	Skip if (CY) = 0	111111	01	—	0011
Subroutine Instructions	CAL ADDR2		Call subroutine	STACK ← (PC) + 1 and PC ← ADDR2	1011	ADDR2 (12 bits)		
	RN		Return to main routine	PC ← (STACK)	111111	10	—	0011
	RNS		Return to main routine and skip unconditionally	PC ← (STACK) and skip	111111	11	—	0011
JUMP Instructions	JUMP ADDR1		Jump to address specified	PC ← ADDR1	10	ADDR1 (14 bits)		
Interruption Instruction	DI		Reset IMF (Note)	IMF ← 0	111111	00	—	0111
	EI		Set IMF (Note)	IMF ← 1	111111	01	—	0111
	RNI		Return to main routine and set IMF (Note)	PC ← (STACK) IMF ← 1	111111	11	—	0111

Note: IMF bits is an interruption master permission flag and is arranged on I/O map.
(→ Refer to the interruption function)

Instruc-tion Group	Mnemonic	Skip Function	Function Description	Operation Description	Machine Language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Other Instructions	SHRC M		Shift memory bits to right direction with carry	0 → (M) b3 → (M) b2 → (M) b1 → (M) b0→ (CY)	111111	DR	DC	0000
	RORC M		Rotate memory bits to right direction with carry	→ (M) b3 → (M) b2 → (M) b1→ (M) b0 → (CY)	111111	DR	DC	0001
	XCH M		Exchange memory bits mutually	(M) b3 ⇔ (M) b0, (M) b2 ⇔ (M) b1	111111	DR	DC	0110
	DAL ADDR3, r		IF DAL bit = 0 then load program in page 0 to DATA register (Note) IF DAL bit = 1 then load program memory referring to DAL address register to DATA register (Note)	DATA ← [ADDR3 + (r)] p in page 0	111110	ADDR3 (6 bits)		RN
	WAIT P		At P = "0" H, the condition is CPU waiting (Soft wait mode) At P = "1" H, expect for clock generator, all function is waiting (Hard wait mode)	Wait at condition P	111111	P	—	0100
	CKSTP		Clock generator stop	Stop clock generator to MODE condition	111111	—	—	0101
	NOOP		No operation	—	111111	—	—	1111

Note: The lower four bits among the ten-bit address of the program memory specified with the DAL instruction (DAL ADDR3 and r) are addressed indirectly with the contents of the general register.

Note: The execution period for the DAL instruction is two machine cycles

Note: DAL bit and DAL address register (DA) are arranged on I/O map.
(→ Refer to the register port item)

Note: When "1" is set to DAL bit and DAL instruction is executed, all the operand part becomes invalid and reference address is used for DAL address register (DA). In this case, assign 0, 0 as dummy data for the operand.

I/O Map (IN1 (M, C), IN2 (M, C), IN3 (M, C), OUT1 (M, C), OUT2 (M, C), OUT3 (M, C))

I/O / Code	φL1 OUT1				φL2 OUT2				φL3 OUT3				φK1 IN1				φK2 IN2				φK3 IN3			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	HF	Power control		FM	I/O port 1 pull-down				I/O port 1				IF monitor			0	A/D data				I/O port 1			
		PW0	PW1		PD0	K1	PD2	PD3	-0	-1	-2	-3	BUSY	MANUAL	OVER		AD0	AD1	AD2	AD3	-0	-1	-2	-3
1	Programmable counter 1				A/D control				I/O port 2				IF data 1				A/D data				I/O port 2			
	P0	P1	P2	P3	AD SEL0	AD SEL1	*	STA	-0	-1	-2	-3	F0	F1	F2	F3	AD4	AD5	BUSY	0	-0	-1	-2	-3
2	Programmable counter 2				Serial interface control 1				I/O port 3				IF data 2								I/O port 3			
	P4	P5	P6	P7	edge	$\overline{SCK}$ - INV	$\overline{SCK}$ - I/O	SIO-ON	-0	-1	-2	-3	F4	F5	F6	F7					-0	-1	-2	-3
3	Programmable counter 3				Serial interface control 2				I/O port 4				IF data 3				Serial interface monitor			0	I/O port 4			
	P8	P9	P10	P11	STA	SO - I/$\overline{O}$	8/$\overline{4}$ bit	*	-0	-1	-2	-3	F8	F9	F10	F11	BUSY	COUNT	SIO F/F		-0	-1	-2	-3
4	Programmable counter 4				Serial interface output data 1				I/O port 5				IF data 4				Serial interface input data 1				I/O port 5			
	P12	P13	P14	P15	SO0	SO1	SO2	SO3	-0	-1	-2	-3	F12	F13	F14	F15	SI0	SI1	SI2	SI3	-0	-1	-2	-3
5	Reference select			Programmable counter	Serial interface output data 2				I/O port 6				IF data 5				Serial interface input data 2				I/O port 6			
	R0	R1	R2	P16	SO4	SO5	SO6	SO7	-0	-1	-2	-3	F16	F17	F18	F19	SI4	SI5	SI6	SI7	-0	-1	-2	-3
6	IF counter control 1				Timer reset		CKSTP mode	Test port 2	I/O port 7								Timer				I/O port 7			
	IF1/$\overline{2}$	PW	IF1/$\overline{IN1}$	IF2/$\overline{IN2}$	2 Hz F/F	Clock		#4	-0	-1	-2	-3					2 Hz F/F	10 Hz	100 Hz	0	-0	-1	-2	-3
7	IF counter control 2				Interrupt control				I/O port 8				$\overline{HOLD}$	INTR1	INTR2	0	Interrupt master flag	0	0	0	I/O port 8			
	STA/$\overline{STP}$	MANUAL	G0	G1	POL1 (INTR1)	POL2 (INTR2)	IE	*	-0	-1	-2	-3					IMF				-0	-1	-2	-3
8	MUTE	MUTE control			Interrupt permission flag				I/O port 9				MUTE	MUTE control			Interrupt permission flag				I/O port 9			
		I/O-1	POL	HOLD	EF1 (INTR1)	EF2 (INTR2)	EF3 (SIO)	EF4 (Timer)	-0	-1	-2	-3		I/O	POL	HOLD	EF1	EF2	EF3	EF4	-0	-1	-2	-3
9	UNLOCK Detection	DO2 control			Interrupt latch reset				HOLD PLL off control	IF counter Split	Prescaller IN	PSC ENA	Unlock detection		Input port		Interrupt latch							
	RESET	PN	M0	M1	ILR1 (INTR1)	ILR2 (INTR2)	ILR3 (SIO)	ILR4 (Timer)					F/F	ENA	IN1	IN2	IL1	IL2	IL3	IL4				
A	Buzzer output control 1				Timer counter Interrupt detection data1				DAL	(DATA) → DA	OT Count Up	port 1 Pull-up					Timer counter data 1				DAL	0	0	0
	BF0	BF1	BF2	BEN	ID0	ID1	ID2	ID3									CT0	CT1	CT2	CT3				
B	Buzzer output control 2				Timer counter Interrupt detection data2				DAL address								Timer counter data 2				DAL address			
	BM0	BM1	BUZR ON	POL	ID4	ID5	ID6	ID7	DA0	DA1	DA2	DA3					CT4	CT5	CT6	CT7	DA0	DA1	DA2	DA3
C	CA Flag	*	*	*	Timer counter control				Data register 1				CA flag	0	0	0					Data register 1			
					CK0	CK1	GT	CR	d0	d1	d2	d3									d0	d1	d2	d3
D	G register 1				Data select				Data register 2				G register 1				Data select				Data register 2			
	G0	G1	G2	G3	SEL1	SEL2	SEL4	SEL8	d4	d5	d6	d7	G0	G1	G2	G3	S1	S2	S3	S4	d4	d5	d6	d7
E	G register 2				Segment data 1/ General-purpose output data				Data register 3				G register 2								Data register 3			
	G4	G5	*	*	COM1/OT	COM2/OT	COM3/OT	COM4/OT	d8	d9	d10	d11	G4	G5	0	0					d8	d9	d10	d11
F	Test port 1				Segment data2/ Segment IO control				Data register 4												Data register 4			
	#0	#1	#2	#3	COM1	COM2	COM3	COM4	d12	d13	d14	d15									d12	d13	d14	d15

Refer to the next page

ϕKL2D

Data Select			
S1	S2	S4	S8

I/O / ϕL2D	ϕL2E OUT2 Y1	Y2	Y4	Y8	ϕL2E OUT2 Y1	Y2	Y4	Y8	ϕL3B OUT3 Y1	Y2	Y4	Y8	ϕK3B IN3 Y1	Y2	Y4	Y8
0	S1/OT1~OT4				S17				DAL address 1				DAL address 1			
	COM1 /OT1	COM2 /OT2	COM3 /OT3	COM4 /OT4	COM1	COM2	COM3	COM4	DA0	DA1	DA2	DA3	DA0	DA1	DA2	DA3
1	S2/OT5~OT8				S18				DAL address 2				DAL address 2			
	COM1 /OT5	COM2 /OT6	COM3 /OT7	COM4 /OT8	COM1	COM2	COM3	COM4	DA4	DA5	DA6	DA7	DA4	DA5	DA6	DA7
2	S3/OT9~OT12				S19				DAL address 3				DAL address 3			
	COM1 /OT9	COM2 /OT10	COM3 /OT11	COM4 /OT12	COM1	COM2	COM3	COM4	DA8	DA9	DA10	DA11	DA8	DA9	DA10	DA11
3	S4/OT13~OT16				S20				DAL address 4				DAL address 4			
	COM1 /OT13	COM2 /OT14	COM3 /OT15	COM4 /OT16	COM1	COM2	COM3	COM4	DA12	DA13	*	*	DA12	DA13	0	0
4	S5/OT17~OT18				S21				Pulse counter control				Pulse counter data			
	COM1 /OT17	COM2 /OT18	COM3	COM4	COM1	COM2	COM3	COM4	DOWN	POL	*	*	PC0	PC1	PC2	PC3
5	S6				S22				Pulse counter control				Pulse counter data			
	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4	CTR RESET	OVER RESET	*	*	PC4	PC5	PC6	PC7
6	S7				Segment/IO select								Pulse counter data			
	COM1	COM2	COM3	COM4	S15	S16	S17	S18					OVER	0	0	0
7	S8				Segment/IO select											
	COM1	COM2	COM3	COM4	S19	S20	S21	S22								
8	S9				I/O control 1											
	COM1	COM2	COM3	COM4	-0	-1	-2	-3								
9	S10				I/O control 2											
	COM1	COM2	COM3	COM4	-0	-1	-2	-3								
A	S11				I/O control 4											
	COM1	COM2	COM3	COM4	-0	-1	-2	-3								
B	S12															
	COM1	COM2	COM3	COM4												
C	S13															
	COM1	COM2	COM3	COM4												
D	S14															
	COM1	COM2	COM3	COM4												
E	S15															
	COM1	COM2	COM3	COM4												
F	S16				LCD control			*								
	COM1	COM2	COM3	COM4	DISP OFF	LCD OFF	OTB-UP									

○ I/O map

All of the ports within the device are expressed with a matrix of six I/O instructions (OUT 1 to 3 instructions and IN 1 to 3 instructions) and a 4-bit code number.

The allocation of these ports is shown on the following page in the form of an I/O map. The ports used in the execution of the various I/O instructions on the horizontal axis of the I/O map are allocated to the port code numbers indicated on the vertical axis. The G-register, data register, DAL address register and DAL bits are also used as ports.

The OUT1 to 3 instructions are specified as output ports and the IN 1 to 3 instructions are specified as input ports.

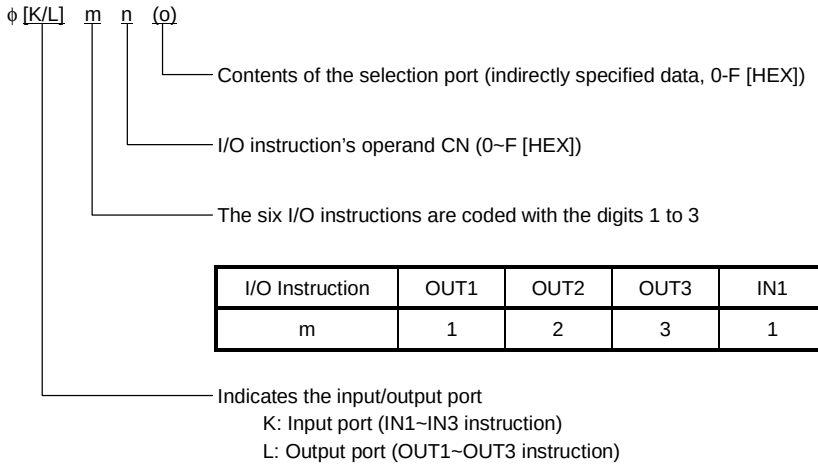
Note: The ports indicated by the angled lines on the I/O map do not actually exist within the device.

The contents of other ports and data memories are not affected when data is output to a non-existent output port with the execution of the output instruction. The data loaded from data memories is unfixed when a non-existent input port has been specified with the execution of an input instruction.

Note: The output ports marked with an asterisk (*) on the I/O map are not used. Data output to these ports assume the don't care's status.

Note: The Y1 contents of the ports expressed in 4 bits correspond to the data memory data's low order bit and the Y8 contents correspond to the high order bits.

The ports specified with the six I/O instructions and code No. C are coded in the following manner:

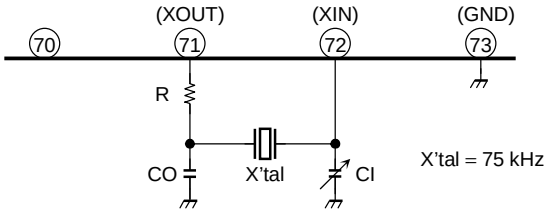


I/O Instruction	OUT1	OUT2	OUT3	IN1	IN2	IN3
m	1	2	3	1	2	3

(Example) The setting for the G-register is allocated to code "D" and "E" in the OUT1 instruction.
The encoded expression at this time becomes "ϕL1D"and "ϕL1E".

○ Crystal Oscillation Circuit

75 kHz crystal oscillator is connected to the device's crystal oscillator pin (XIN, XOUT) as indicated below. Usually, the oscillation signal is supplied to the clock generator, the reference frequency divider and other elements, and generates the various CPU timing signals and reference frequency.



Note: It is necessary to use a crystal oscillator with a low CI value and favorable start-up characteristics. Please adjust and determine external resistance and the constant of a capacitor as the actually used crystal oscillator.

○ System Reset

The device's system will be reset when the $\overline{\text{RESET}}$ pin is subject to the "L" level or when a voltage of 0 V → 0.9 V or more is supplied to the V_{DD} pin (power-on reset). The program will start from 0 address immediately after about 100 ms stand-by time. The $\overline{\text{RESET}}$ pin should be fixed at the "H" level as the power-on reset function is used under normal condition.

Note: A power-on reset function can be forbidden with AI switch. Please specify power-on reset prohibition and use in ES order request sheet. In case of forbidden the power-on reset function, reset with a $\overline{\text{RESET}}$ pin.

Note: The LCD common signal and the segment output will be fixed at the "L" level during system reset and the subsequent stand-by period.

Note: Among the internal port shown in the above I/O map, the port which is not initialized after the system reset should be initialized by the program. The inside port on the I/O map, the port or bit with ◣ mark on I/O map is set to "0" after system reset and the port or bit with ◤ mark is set to "1". The port or bit with no mark is unfixed.

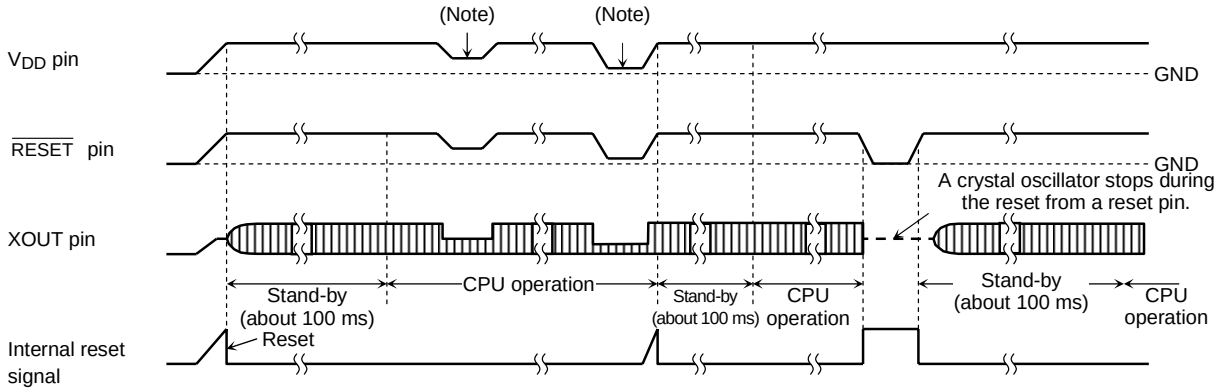
I/O \	ϕL2F			
	OUT2			
ϕL2D	Y1	Y2	Y4	Y8
8	I/O control -1			
	-0	-1	-2	-3

After system reset, this port is set to "0".

I/O \	ϕL1			
	OUT1			
Code	Y1	Y2	Y4	Y8
5	Reference select			Programmable counter
	R0	R1	R2	P16

After system reset, this port is set to "1".

After system reset, this bit is unfixed.



<Timing of operation>

Note: When power supply voltage may become below 0.9 V, set up the clock stop mode or operate the reset function. The CPU operations are reset when a power supply voltage is re-apply from 0.3 to 0.6 V. (Power-on reset)

○ Back-up Mode

By executing CKSTP instruction or WAIT instruction, three kinds of back-up mode can be activated.

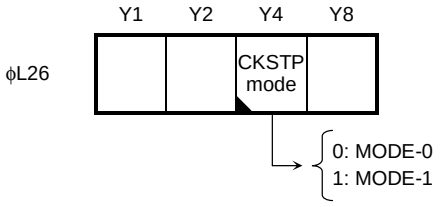
1. Clock Stop Mode

The clock stop mode is a function that suspends system operations and maintains the internal status immediately prior to suspension at a low level of current consumption (under 1 μA). Crystal oscillations suspend simultaneously and CMOS output ports and output pins for LCD display are automatically fixed at the "L" level and N-channel open drain pins are fixed off status (high impedances) automatically. The supply voltage can be reduced to 0.75 V with the clock stop mode.

Suspension is activated at the CKSTP instruction execution address when the CKSTP instruction is executed. The next address is executed after approximately 100 ms of stand-by time when the clock stop mode is cancelled.

(1) Clock stop mode setting

There are two types of mode setting for the clock stop mode. The required setting is selected with the CKSTP MODE bit. This bit is accessed with the OUT2 instruction for which [CN = 6H] has been specified in the operand.



① MODE-0

By setting this mode, the clock stop mode is assumed if the CKSTP instruction is executed when the $\overline{\text{HOLD}}$ pin is in the "L" level. The same operations as the NOOP instruction will be assumed if the CKSTP instruction is executed when the $\overline{\text{HOLD}}$ pin is in the "H" level.

② MODE-1

By setting this mode, the clock stop mode is assumed when the CKSTP instruction is executed regardless of the $\overline{\text{HOLD}}$ pin level.

Note: PLL will assume the off status during CKSTP instruction execution.

Note: Before the execution of the clock stop instruction, be sure to access $\overline{\text{HOLD}}$ input pin and I/O port 1 input port and reset the 2 Hz F/F. If the clock stop mode is executed without executing the instruction, it may not be the mode.

(2) Canceling the clock stop mode

① MODE-0

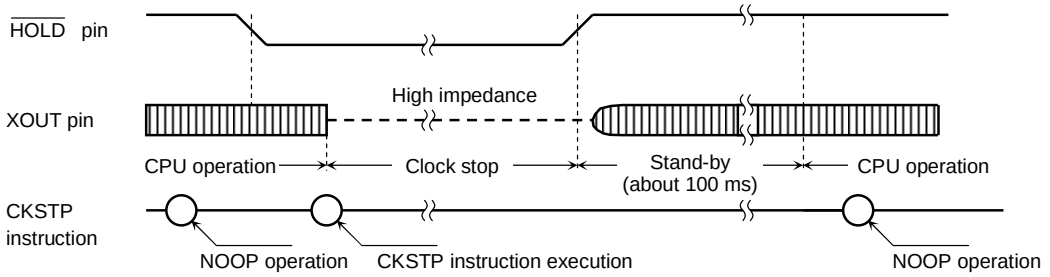
The clock stop mode is cancelled when specified in this mode by changing the "H" level of the $\overline{\text{HOLD}}$ pin or the input status of I/O port (P1-0~3) specified in the input port.

② MODE-1

The clock stop mode is cancelled when specified in this mode by changing the $\overline{\text{HOLD}}$ pin or the input status of I/O port (P1-0~3) specified in the input port.

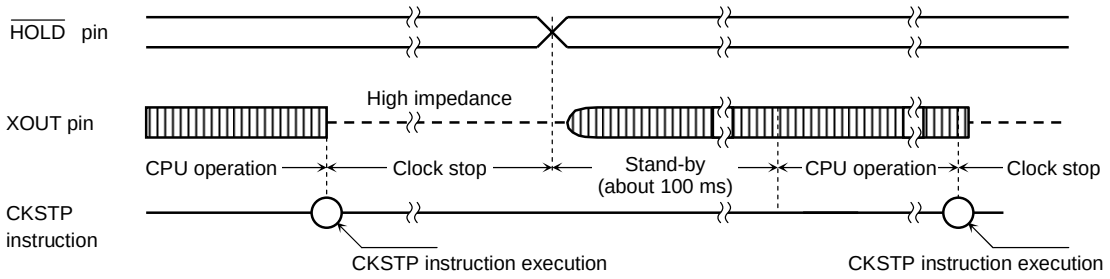
(3) Clock stop mode timing

① MODE-0



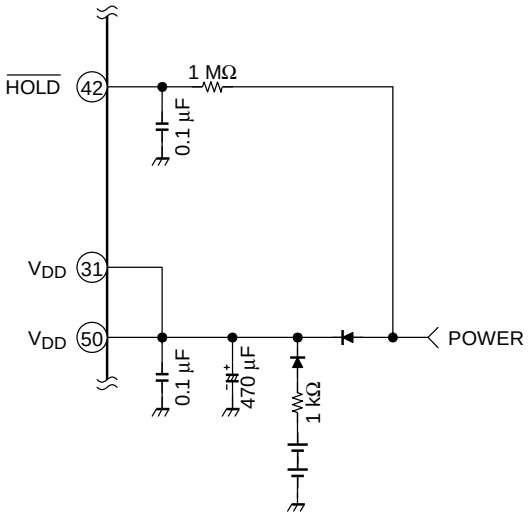
(The clock stop mode is assumed when the CKSTP is executed during the "L" level of the $\overline{\text{HOLD}}$ input.)

② MODE-1

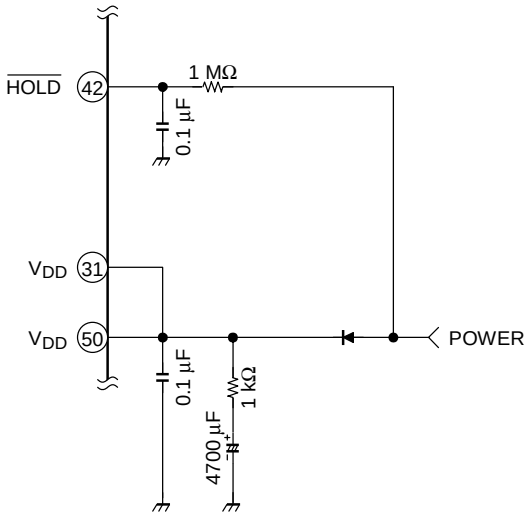


(The clock stop mode is assumed whenever the CKSTP instruction is executed.)

(4) Example of a back-up circuit (example of a MODE-0 circuit)



Example of a battery back-up circuit



Example of a capacitor back-up circuit

2. Wait Mode

The wait mode suspends system operations, maintains the internal status immediately prior to suspension and reduces current consumption. There are two types of wait mode available; the SOFT WAIT mode and the HARD WAIT mode. It is suspended at the address of the WAIT instruction execution when the WAIT mode is activated. The next address is executed immediately after the wait mode is cancelled without entering a stand-by status.

(1) SOFT WAIT mode

Only the CPU operations within the device are suspended when the WAIT instruction in which [P = 0H] has been specified in the operand is executed. The crystal resonator and other elements will continue to operate normally at this time. The SOFT WAIT mode is efficient in reducing current consumption during clock operations used in programs that include clock functions.

Note: Current consumption will differ in accordance with execution time of CPU operation.

(2) HARD WAIT mode

The operations of all elements, with the exception of the crystal resonator, can be suspended by the execution of the WAIT instruction in which [P = 1H] has been specified in the operand. This enables even greater levels of current consumption reduction than the SOFT WAIT mode. It suspends the CPU operation.

Note: The output port is maintained during the HARD WAIT mode. All LCD display output pin are fixed "L" level and voltage doubler circuit (V_{DB}), constant voltage circuit for LCD (V_{EE}) and voltage doubler circuit for LCD (V_{LCD}) are operated.

(3) Wait mode setting

The wait status is assumed whenever the WAIT instruction is executed.

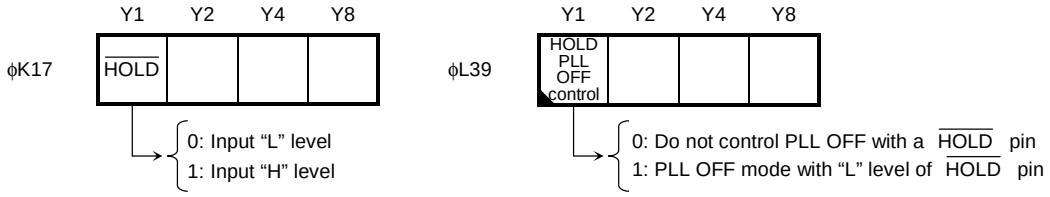
Note: The PLL OFF status will be assumed during the wait mode.

(4) Wait mode cancellation conditions

The wait mode is cancelled when the following conditions are fulfilled:

① When the input status of the $\overline{\text{HOLD}}$ pin changes.
② When the input status of the I/O port specified in the input port (P1-0~3) changes.
③ When the 2 Hz Timer F/F is set to "1" (only with the SOFT WAIT mode)

3. $\overline{\text{HOLD}}$ Input Port



The $\overline{\text{HOLD}}$ pin can be used as an input port. This bit loads data input with IN1 instruction for which [CN = 7H] has been specified in the operand into the data memory. It is necessary to access this port prior to the execution of the Back-up instruction when the clock stop mode or WAIT mode has been set. It is necessary to note that there are cases when the clock stop mode will not be activated if the Back-up instruction is executed without this port being accessed.

While HOLD PLL off control bit is set to "1", if $\overline{\text{HOLD}}$ pin input "L" level, it will become PLL off-mode. For this reason, a setup in PLL off-mode can be made quickly at the time of battery exchange.

The bit is accessed with the OUT3 instruction for which [CN = 9H] has been specified in the operand. All of the reference port is "1", it also becomes PLL off mode. (→ Refer to the reference frequency divider item)

○ Interrupt Function

The peripheral hardware which can use Interrupt function has INTR1 pin, INTR2 pin, Timer counter, and Serial interface.

The peripheral hardware fulfill conditions, Interrupt demand signal from peripheral hardware is all input, and Interrupt demand is transmitted. When it is received, it branches out vector address determined by each Interrupt factor. Each Interrupt processing routine is started. The pretreatment for returning to the same state as the time of Interrupt, before and after usually carrying out Interrupt processing, and post-processing are required of Interrupt routine. It is necessary to perform shunting and a return for the register data memory used by ALU to the data memory for interchange. When ending Interrupt processing, a program is returned by the return command for Interrupt.

1. Interrupt Control Circuit

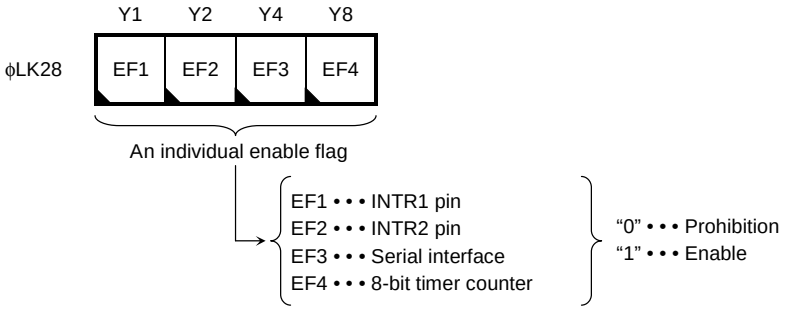
Interrupt control circuit consists of an Interrupt enable flag, an Interrupt latch, and an Interrupt priority circuit block. This control performs setup and control by OUT2/IN2 instructions.

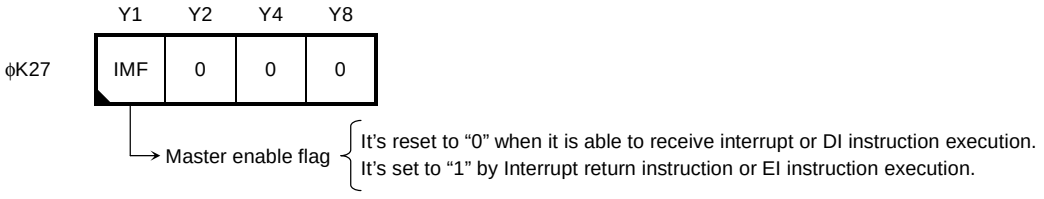
(1) Interrupt enable flag

Interrupt enable flag has an individual permission flag corresponding to a master permission flag and each Interrupt factor. An individual enable flag sets up prohibition/permission of Interrupt corresponding to each Interrupt factor. A master enable flag is a flag for which performs prohibition/permission of all Interrupts. If these enable register is set to "1", it becomes permission and is set to "0", it becomes prohibition. An individual enable flag is accessed with OUT2/IN2 instructions for which [CN = 8H] has been specified to the operand. A master enable flag can perform permission/prohibition by execution of an EI/DI instruction. A master enable flag is a flag which performs prohibition/permission of all Interrupts. If these enable register is set to "1", it becomes enable and is set to "0", it becomes prohibition.

In case of forbidding Interrupt in a program, it executes DI instruction, and in case of enabling, it executes EI instruction. At this time, Interrupt is enabled during the EI instruction execution in a program, and the DI instruction execution.

If master enable flag is received the Interrupt request, it is reset by "0" and all Interrupts will be in a prohibition state. By executing of Interrupt return instruction, it is set to "1". A master enable flag is read into data memory by IN2 instruction for which [CN = 7H] has been specified.



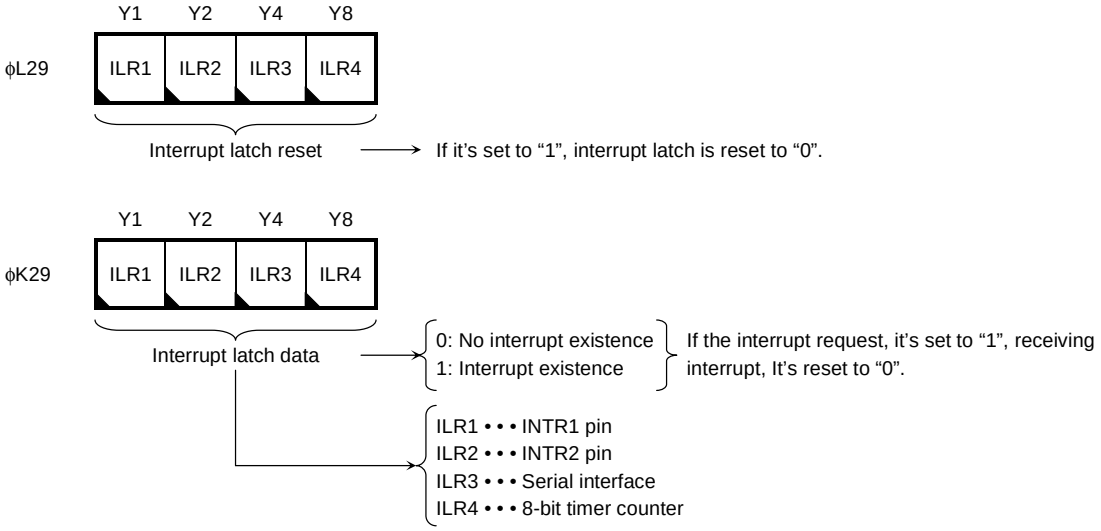


(2) Interrupt latch

If Interrupt request generates, interrupt latch is set to “1”.

If Interrupt is enabled, Interrupt reception will be required of CPU and it will branch Interrupt routine. If Interrupt is received at this time, Interrupt latch is reset by data “0” automatically.

Interrupt latch data can read by the program and judge individual existence or nothing of interrupt generating. By interrupt request, interrupt latch is reset from “1” from setting “0”, it is able to cancel interrupt request or initialization.



(3) Interrupt priority circuit block

Interrupt priority circuit is a circuit of determined the ranking of the interrupt generating when interrupt occurs simultaneously or interrupt permit after two or more interrupts had occurred. Vector address to interrupt routine is also generated by this block.

Priority	Interrupt Factor	Vector Address
1	INTR1 pin	0001H
2	INTR2 pin	0002H
3	Serial interface	0003H
4	Timer counter	0004H

2. Interrupt Reception Processing

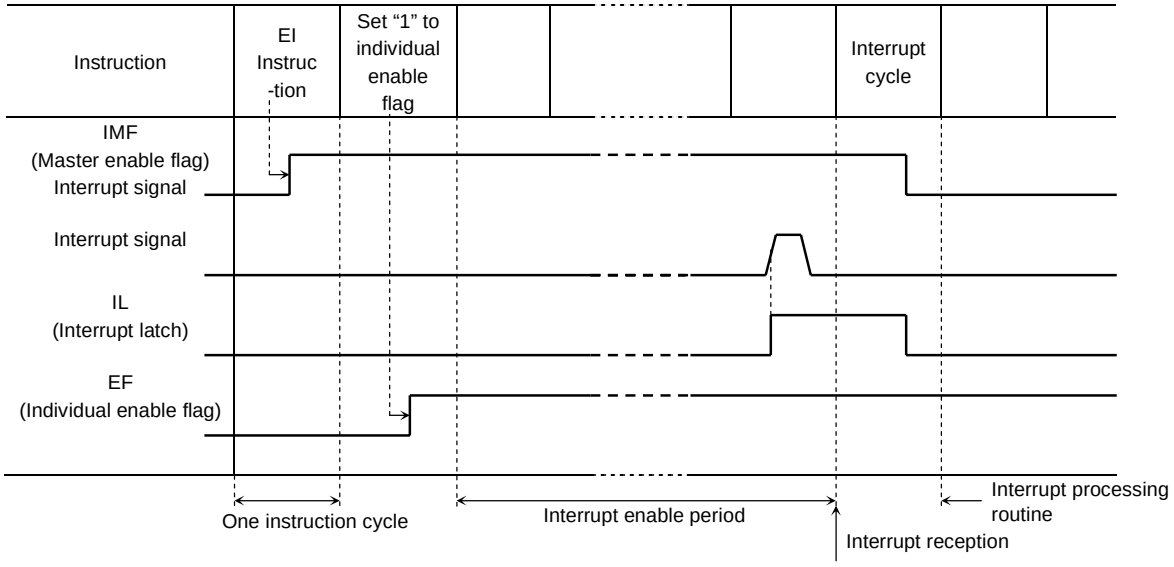
Interrupt request is maintained until it receives interrupt or reset to "0" to interrupt latch by system reset operation or by the program. Interrupt reception operation is as shown below.

① Each peripheral hardware is output each interrupt signal and set to "1" to interrupt latch if interrupt conditions are fulfilled.
② Interrupt latch of Interrupt factor received resets to "0" if interrupt enable flag and the master enable flag corresponding to each Interrupt factor set to "1"
③ Interrupt master enable flag resets to "0" and interrupt is forbidden.
④ The contents of a stack pointer are -1.
⑤ The contents of program counter (PC) evacuates stack register. At this time, the contents of a program counter become the following address, which permitted the next address or next interrupt at the time of interrupt being received.
⑥ The contents of vector address corresponding to received interrupt transfers to program counter.
⑦ Executes the contents of vector address.

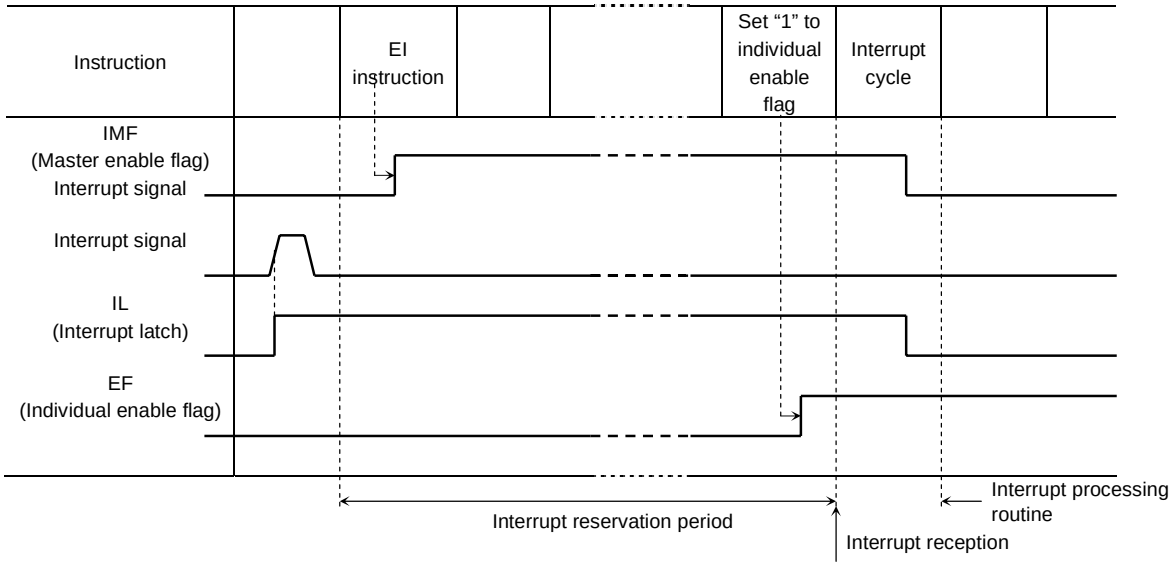
These executions ①~⑥ are executed during 1 instruction cycle. The instruction cycle is called "Interrupt cycle".

Note: Stack pointer is the pointer which specifies the 8-level stack register. Reference of the contents of a stack pointer cannot be performed.

In case of Interrupt enable period



In case of interrupt reservation period



3. Return Processing from Interrupt Processing Routine

In order to make it return to processing before receiving Interrupt from Interrupt processing routine, RNI instruction which is an exclusive command is used.

Execution of RNI instruction follows the processing automatically one by one.

① The contents of address stack, which is specified with a stack pointer, are returned to a program counter.
② Set "1" to interrupt master enable and changes into an enable state.
③ The contents of a stack pointer are done +1.

RNI instruction of the above-mentioned processing is processed in 1 instruction cycle.

4. Interrupt Processing Routine

Interruption is received regardless of the program currently performed when an interruption request will be done if it is the program area where interruption is enabled. Therefore, after doing interrupt processing, when making it return to the program of a basis, it is necessary to return to the state where it is performed by interrupt processing. For this reason, it is necessary to perform shunting and return operation within an interruption processing routine about a register, a data memory, etc. which may be operated within an interruption processing routine at least.

(1) Shunting processing

In execution of shunting processing, a carry flag surely needs to be shunted. If interruption is received during execution of arithmetic operation, the contents will change about carry flag (CY) etc. and the program after a return will mistake judgment. For this reason, the contents of a carry flag are shunted in a data memory at once by IN1 instruction in the data of the carry flag in I/O map.

The contents of the data memory used by the interruption processing routine and the contents of a general register are also made to shunt if needed. Furthermore, when MVGD, MVGS or DAL instruction is used in interrupt routine, it's necessary to shunt the contents of G-register or DAL address register.

(2) Return processing

Return processing should just do opposite to the above-mentioned shunting processing.

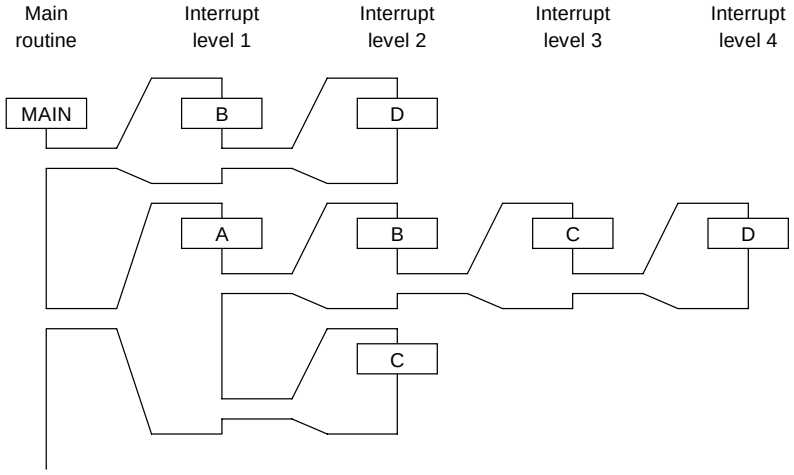
If interrupt is received, interrupt master enable flag is reset by "0", before receiving interrupt, an interrupt master enable flag must have been "1".

For this reason, RNI instruction is executed and a master enable flag is returned.

5. Multiplex Interrupt

Multiplex Interrupt is the method of processing another interrupt during interrupt processing.

As shown in the figure, another interrupt factor C or D is processed during interrupt processing to a certain interrupt factor A and B. The depth of interrupt at this time is called interrupt level.



The example of multiplex interrupt

Note the following points when using multiplex interrupt.

① The priority of interrupt factor
② Restriction of the address stack level used at the time of interrupt request issue
③ Shunting processing of a carry flag, a data memory, etc.

(1) Priority of interrupt factor

The priority of multiplex interrupt is A < B < C < D in the figure. In this priority, interrupt of C must be processed prior to interrupt of A or B even if it is under processing and even if interrupt of C is under processing, interrupt of D must be given priority.

For example, there are interruption factors A and B, it assumed that the factor of A requests every 10 ms and the interrupt processing time is 4 ms and the factor of B requests every 2 ms and the interrupt processing time is 1 ms. When there is no priority of A and B, if an interrupt requests of A enters during interrupt processing of B interrupt, processing of A is done and it will stop doing interrupt processing of B. In such a case, it is necessary to program that give the priority of A < B and forbid interrupt of A during interrupt processing of B, and even if interrupt of B is received under processing of interrupt of A.

When all individual enable flags is setup "1" (enable state), it becomes the priority by the hardware explained according to the item of an interrupt priority circuit block, the priority of hardware is changeable by operating an individual enable flag by the program.

Usually, in interrupt processing routine, received interrupt and low priority interrupt is forbidden and high priority interrupt of Interrupt is enabled.

(2) Restriction of address stack level

As the item of Interrupt reception processing explained, when interrupt request was done, the return address is shunted automatically to address stack. As the register item explained, an address stack is used also for execution of a sub routine call instruction on eight levels. For this reason, if interrupt level and a sub routine call level exceed eight levels, it returns and the contents of an address stack which was recorded from the first will be destroyed, it is necessary to use it so that this may not be exceeded.

(3) Shunting processing

When using multiplex interrupt, it is necessary to secure the shunting area of shunting processing separately to each Interrupt factor.

○ External Interrupt and Timer Counter Function

External interrupt has two types of INTR1 pin and INTR2 pin. Interrupt request is done by the rising or falling edge of a signal added to these pins.

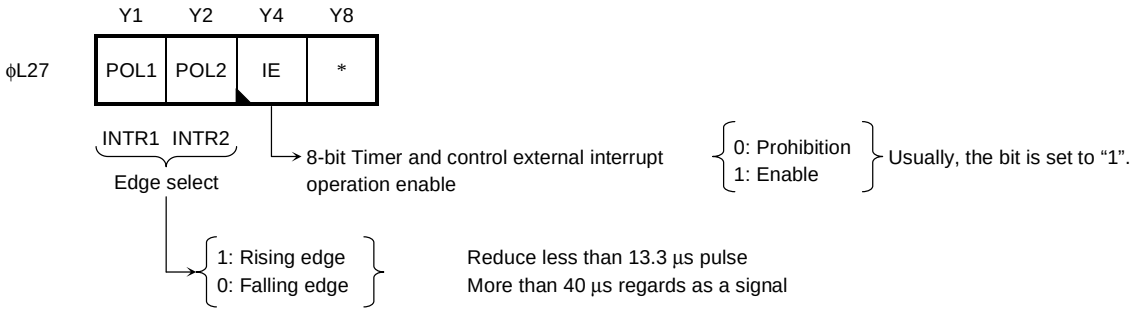
Timer counter is 8-bits binary counter and has the function of timer and external clock timer. The input of external clock timer function is used as external interrupt pin (INTR1, INTR2).

1. External Interrupt Function

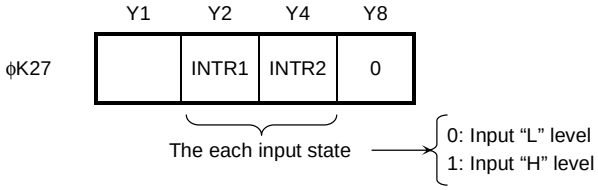
External interrupt has two types of INTR1 pin and INTR2 pin and the edge of these inputs is detected and Interrupt request is done. Input has noise cancel circuit, the frequency of 75 kHz is used for a noise removal clock and the pulse of under this frequency is removed as a noise. IE bit is enable bit which permits 8-bit timer counter operation or interrupt and external interrupt request. The rising or falling edge used as input edge can choose for every pin. Usually, this bit is set "1".

These controls are accessed with OUT2 instruction for which [CN = 7H] has been specified in the operand. If Interrupt of INTR1 pin is received, the program will branch to 0001H address and a program will branch to 0002H address at the time of INTR2 pin.

These pins are used as input port and the input status can read into data memory by execution of the IN2 instruction for which [CN = 7H] has been specified in the operand.



Note: The edge of the external clock of timer counter is also controlled. The Timer counter input is not used the function of noise cancel function. For this reason, even if external Interrupt does not occur, it is 40 (since the clock pulse of under s is inputted into counter, cautions are required.).



Note: Interrupt request may be transmitted if edge is changed by POL bits. For this reason, when changing edge, it changes after forbidding Interrupt, and Interrupt latch is reset, and it returns to usual operation.

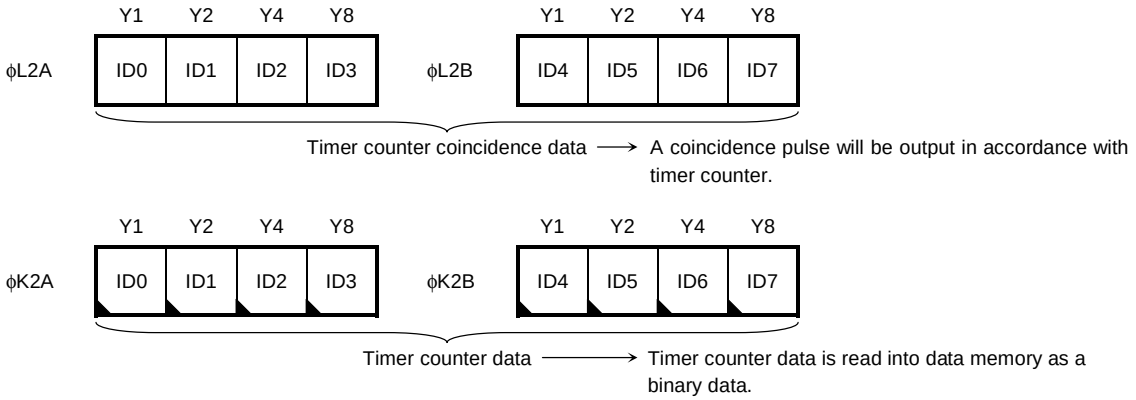
2. Timer Counter Function

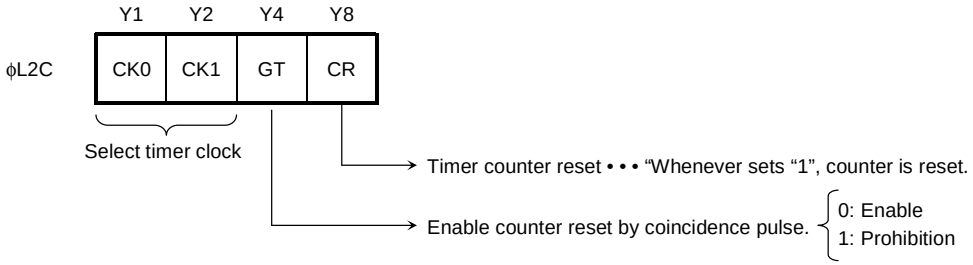
Timer counter are consists of 8-bit binary counter, counter coincidence register, digital comparator and controlled the control circuit.

If timer counter is coincided with the contents of counter coincidence register, timer counter is outputted a coincidence signal pulse and interrupt request is done by inputting timer clock to 8-bit binary counter timer clock. Reset of Timer counter is possible with a coincidence pulse and a program, and it can perform enable and prohibition of reset by the coincidence pulse. As a clock of timer, it can be selected INTR1/2 input and an instruction cycle and 1 kHz.

(1) Timer counter register configuration

The register of timer counter consists of counter data, coincidence register and control register.





CK0	CK1	Timer clock
0	0	INTR1 pin input
0	1	INTR2 pin input
1	0	Instruction cycle clock (40 μs)
1	1	1 kHz

Select clock edge by POL bit
0: Count by raising edge
1: Count by falling edge

Note: It's necessary to set "1" to IE bit when it uses timer counter.

(2) Timer mode

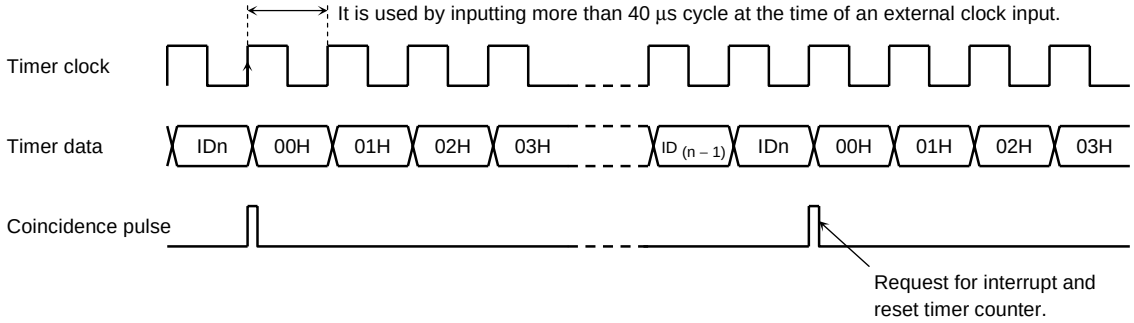
Timer mode is detected fixed time. Interrupt request is done and reset to counter whenever it detects fixed time. At this time, control bit is set to 1 kHz or an instruction as timer clock, "0" to GT bit and "0" (it does not reset) to CR bit.

Timer coincidence data is

Timer time = IDn (coincidence data) × Timer clock cycle

It sets up the data which corresponding to time.

In addition, although an external pin can be used for Timer clock, a clock frequency should use the frequency below 25 kHz. If GT bit is setup "1", it can also be integrated of an external clock.



○ Internal Interrupt and Interrupt Function

Interrupt has two types of timer counter and serial interface.

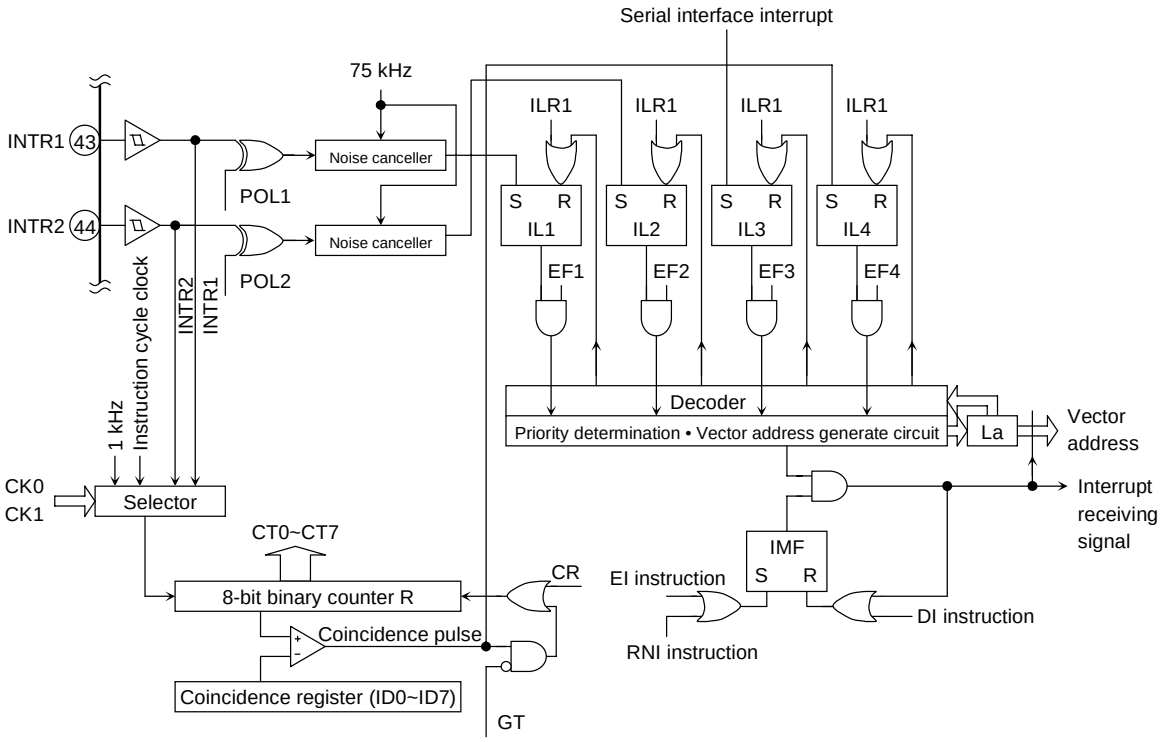
1. Interrupt of Timer Counter

If timer counter value is the same as coincidence register value, interrupt of timer counter is transmitted interruption. Refer to the item of timer counter function for details.

2. Interrupt of Serial Interface

Interrupt of serial interface is transmitted interruption at the time of finishing operation of serial interface. Refer to the item of serial interface function for details.

3. Interruption Block Configuration



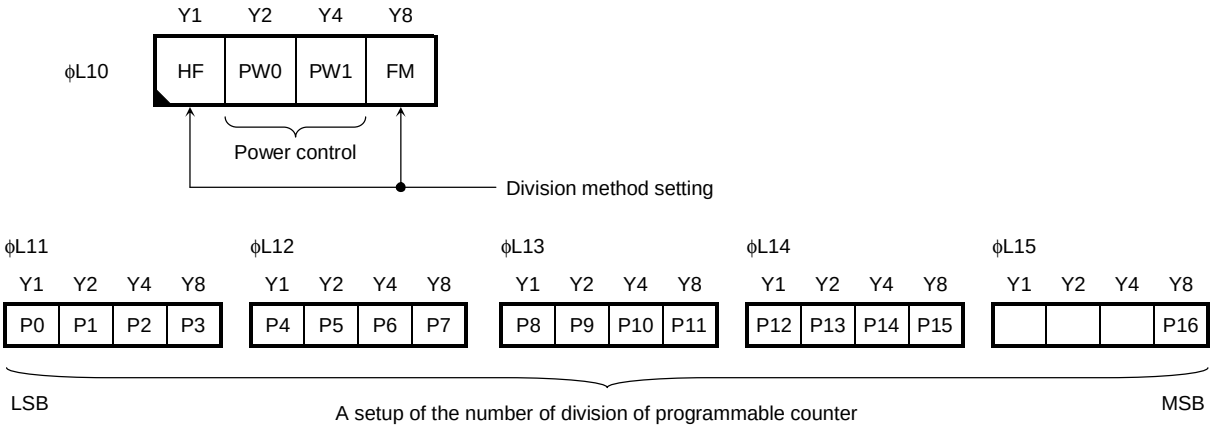
○ Programmable Counter

The programmable counter consists of two modulus prescaller, a 4-bit + 13-bit programmable counter and a port to control these elements.

The programmable counter controls the ON/OFF functions for the contents of the reference port and $\overline{\text{HOLD}}$ input status. By using external prescaller (TD6134AF/TD7101/04F) or 1 chip tuner IC that is built-in for 1/16 prescaller (TA2142FN), it's possible to reduce the emission from the tuner portion and consumption current.

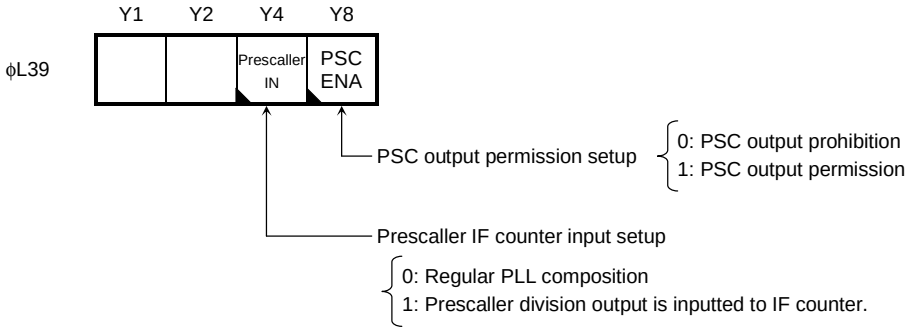
1. Programmable Counter Control Port

This port is controlling for division frequency, division method and operating current and gain of prescaller.



The division method and power control of prescaller are accessed with the OUT1 instruction for which [CN = 0H] has been specified in the operand.

The division frequency setting is accessed with the OUT1 instruction for which [CN = 1~5H] has been specified and setting is by writing in the P16 bit (ϕL15). All data between P0 to P16 are updated when P16 is set. It is therefore necessary to access P16 even when updating only certain items of data and to perform setting as the final process.



PSC output permission setup is used at the time of connection of external prescaller.

In the setup to prescaller IF input, if the bit is set to "1", a programmable counter stops and prescaller 1/15 and 16 are fixed to 16 division. Usually, consisting of PLL, the bit is set to "0".

(→ Refer IF counter item)

2. Division Method Setting

The pulse swallow method or direct method are selected with the HF and FM bit.

The power control bits (PW0/1) are controlled the gain of amplifier and prescaller (1/2 + 1/15・16). Although the power bit in each mode has five methods, set up it as shown in the table.

By using 1 chip tuner IC that is built-in for 1/16 prescaller (TA2142FN), set up to the LF mode and set the division value after 1/16 division frequency.

Mode	HF	PW0	PW1	FM	Division Method	Example of Receiving Band	Operation Frequency Range	Input Pin	Division Number (Note)
LF	0	1	0	0	Direct division method	MW/LW	0.5~8 MHz	AMin	n
HF1	1	1	0	0	Pulse swallow method (1/15•16)	SW	3~30 MHz		
HF2	1	0	1	0			1~10 MHz		
FM	1	1	0	1	Pulse swallow method (1/2 + 1/15•16)	FM	30~130 MHz	FMin	2•n
VHF	1	0	1	1		TV (1 ch~12 ch)	50~230 MHz		

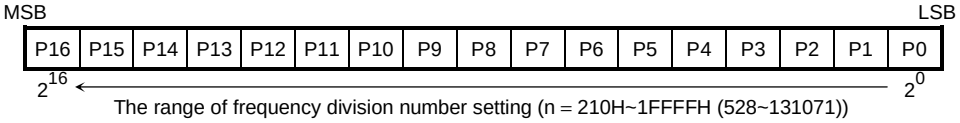
Note: "n" represents the number of divisions programmed.

Note: It may not operate normally with abnormal current dissipation or unlocked PLL etc.

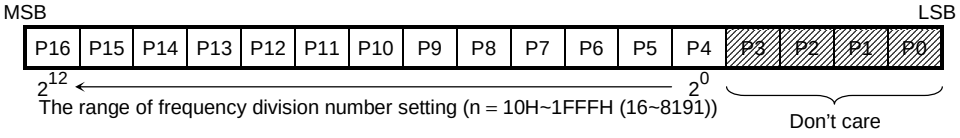
3. Frequency Division Number Setting

The frequency division number for the programmable counter is set in bits P0 to P16 in binary.

- Pulse swallow method (17 bits)

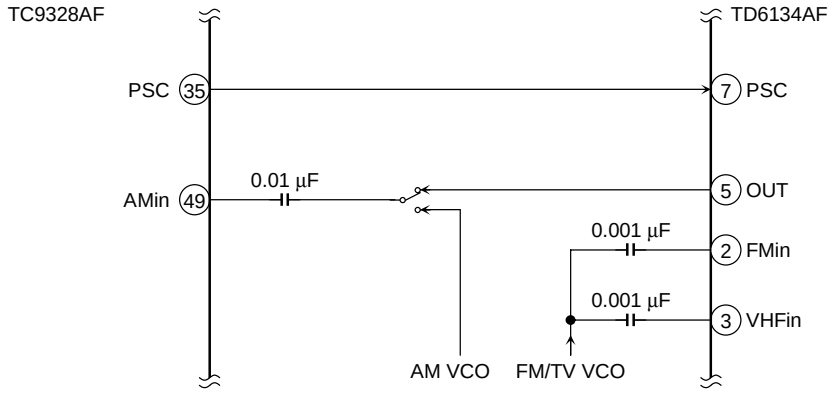


- Direct division method (13 bits)



4. PSC Output Permission Setting

In case of using the external pre-sccaler (TD6134AF/TD7101/04F), PSC output permission bit is setup to "1". At this time, a swallow counter will be operating and prescaller will be in a stop state, and PSC output is outputted P2-3 pin. A division method is set as LF mode, and AM VCO input and an external prescaller output are changed and inputted into AMin input pin. P2-3 pin is used by setting it as an output port.

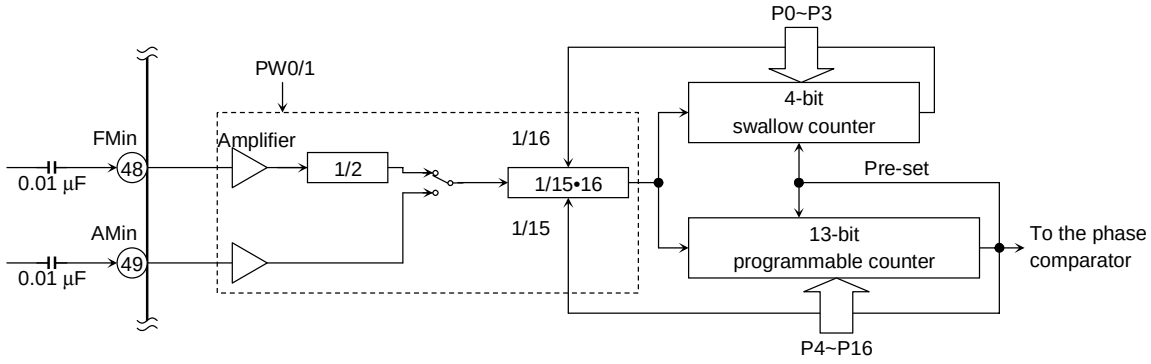


The example of an external prescaller connection circuit

5. Programmable Counter Circuit Configuration

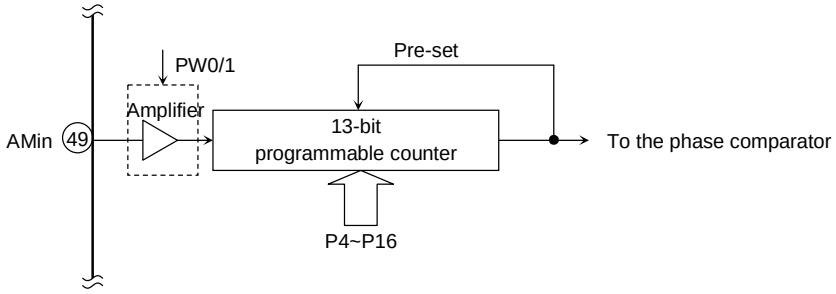
- Pulse swallow method circuit configuration

This circuit consists of amplifier, 1/2 prescaller, two 1/15・16 modulus prescallers, the 4-bit swallow counter and a 13-bit binary programmable counter. A 1/2 frequency divider is added to the front stage of the prescaller in the VHF/FM mode.



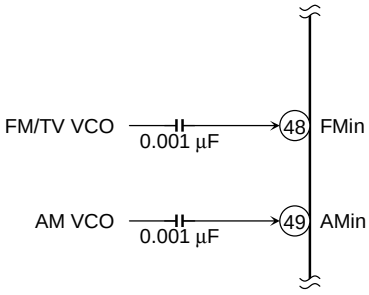
- Direct division method circuit configuration

  The prescaller is not required if this is selected, and instead, the13-bit programmable counter is used.

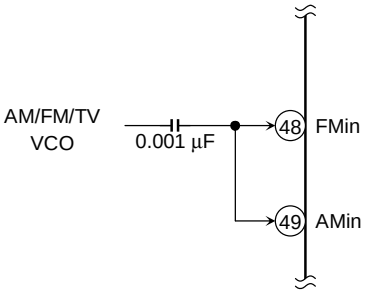


Note: FMin and AMin contain the amplifier, and small-size width operation can be performed by connecting them to a capacitor. In the division method, when non-selected input pins are in PLL off mode, the input becomes high impedance. Therefore FMin and AMin can be used as wired-OR configuration as shown below.

Note: If it becomes PLL off-mode, all programmable counter parts will be stopped. The contents of each control port are held at this time.



The example of connection circuit using VSO for each FM and AM band



The example of connection circuit using VSO with FM and AM bands

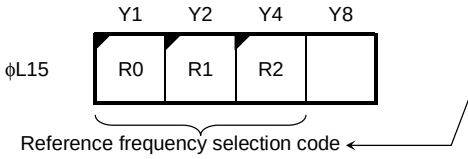
○ Reference Frequency Divider

The reference frequency divider divides the oscillation frequency of the external 75-kHz crystal and generates the following seven types of PLL reference frequency signals; 1 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.25 kHz, 12.5 kHz and 25 kHz. These signals are selected with reference port data.

The selected signal is supplied as a reference frequency for the phase comparator as described below. Also, the PLL is switched on and off with the contents of the reference port.

1. Reference Port

The reference port is an internal port for selecting the seven reference frequency signals. This port is accessed with the OUT1 instruction for which [CN = 5H] has been specified in the operand (ϕL15). Operations for the programmable counter, the If counter, reference counter and the phase comparator are suspended and the PLL assumes the off mode when the contents of the reference port are all "1". As the frequency division setting data for the programmable counter is updated when the reference port is set, it is necessary to set the frequency division number of the programmable counter prior to setting the reference port.



R2	R1	R0		Reference Frequency
0	0	0	0	1 kHz
0	0	1	1	3 kHz
0	1	0	2	3.125 kHz
0	1	1	3	5 kHz
1	0	0	4	6.25 kHz
1	0	1	5	12.5 kHz
1	1	0	6	25 kHz
1	1	1	7	PLL off mode

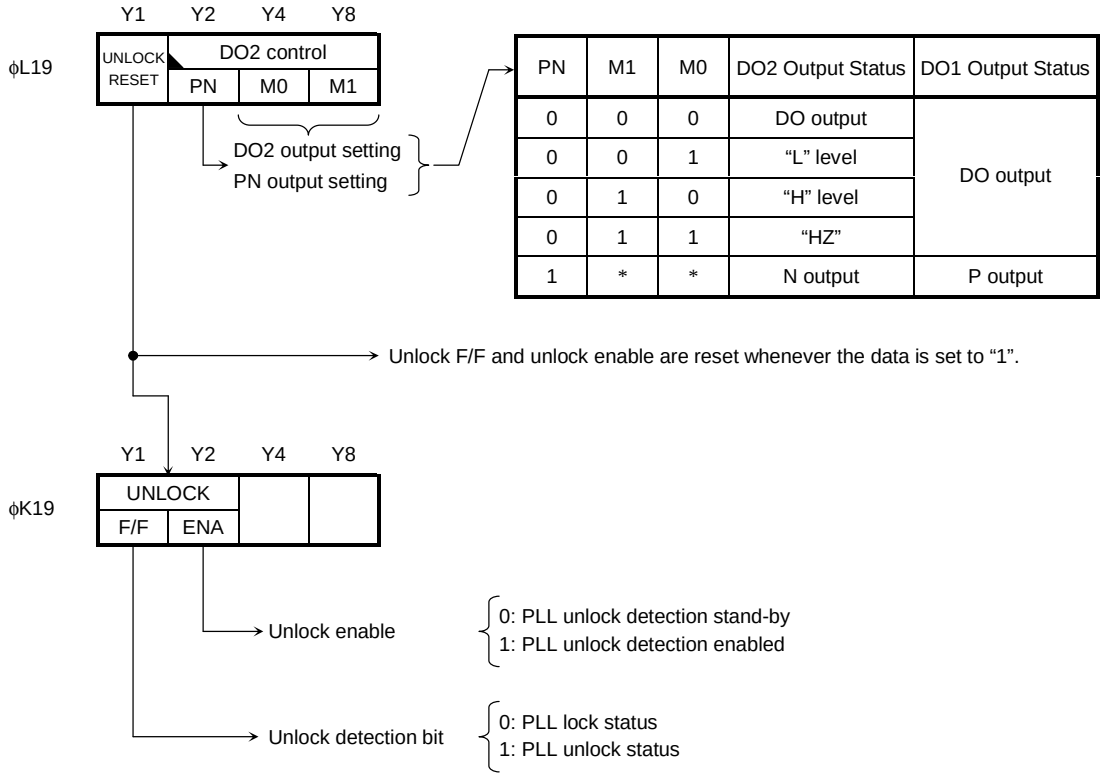
○ Phase Comparator and Lock Detection Port

The phase comparator compares the difference in phasing between the reference frequency signal supplied from the reference frequency divider and frequency division output of the programmable counter and outputs the result. Then it controls the VCO (Voltage control oscillator) via a low pass filter in order to ensure that the two frequency signals and the phase difference match.

Two tristate buffer DO1 and DO2 are outputted in parallel from the phase comparator, the filter constant can be designed for each VHF and AM bands. A charge pump output uses constant voltage V_{reg} potential (1.5 V) so that a stabilized phase comparison machine can be used when V_{DD} potential is 0.9 V.

Also DO2 pin can be used with DO2 control port as general-purpose output port and charge pump signal (P, N) can be outputted from DO1 and DO2 pins. Therefore it is possible to use an external charge pump.

1. DO1 control Port and the Unlock Detection Port



PN	M1	M0	DO2 Output Status	DO1 Output Status
0	0	0	DO output	DO output
0	0	1	"L" level	
0	1	0	"H" level	
0	1	1	"HZ"	
1	*	*	N output	P output

M0 and M1 bit of DO2 control ports perform a general-purpose output port setup of DO2 output, and a setup of high impedance. PN bit performs control setup of an external charge pump for DO1/2 pins as P/N output.

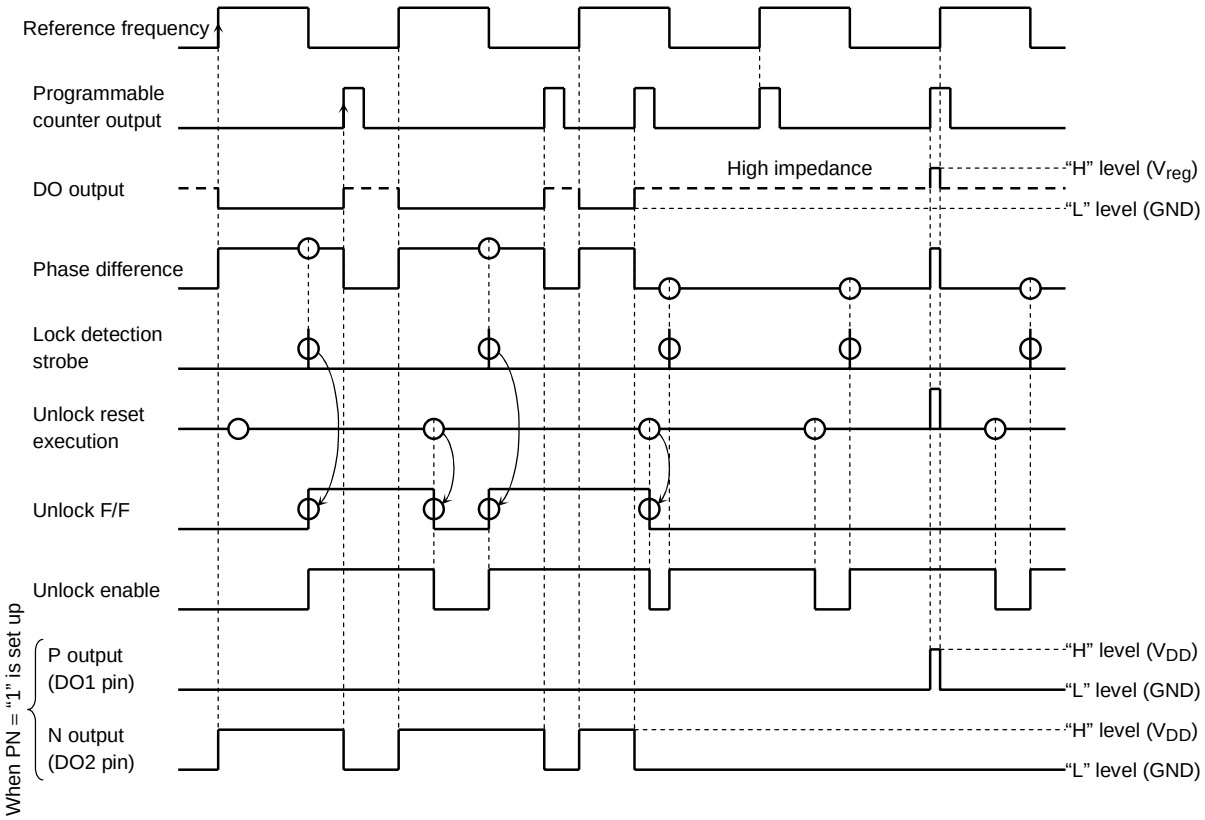
Unlock F/F detects the phase difference of a programmable counter division output and reference frequency to the timing from which about 180 degrees of phases shifted. When a phase does not suit at this time (that is unlock status), unlock F/F is set. The unlock F/F status is reset whenever the UNLOCK RESET bit is set to "1".

It is necessary to access to UNLOCK F/F after establishing more time than is required for the reference frequency cycle after the unlock F/F has been reset in order to detect the phase difference with the reference frequency cycle. It is for this purpose that the enable bit has been made available, but the unlock F/F must not be accessed before it has been confirmed that the unlock enable has been set at "1".

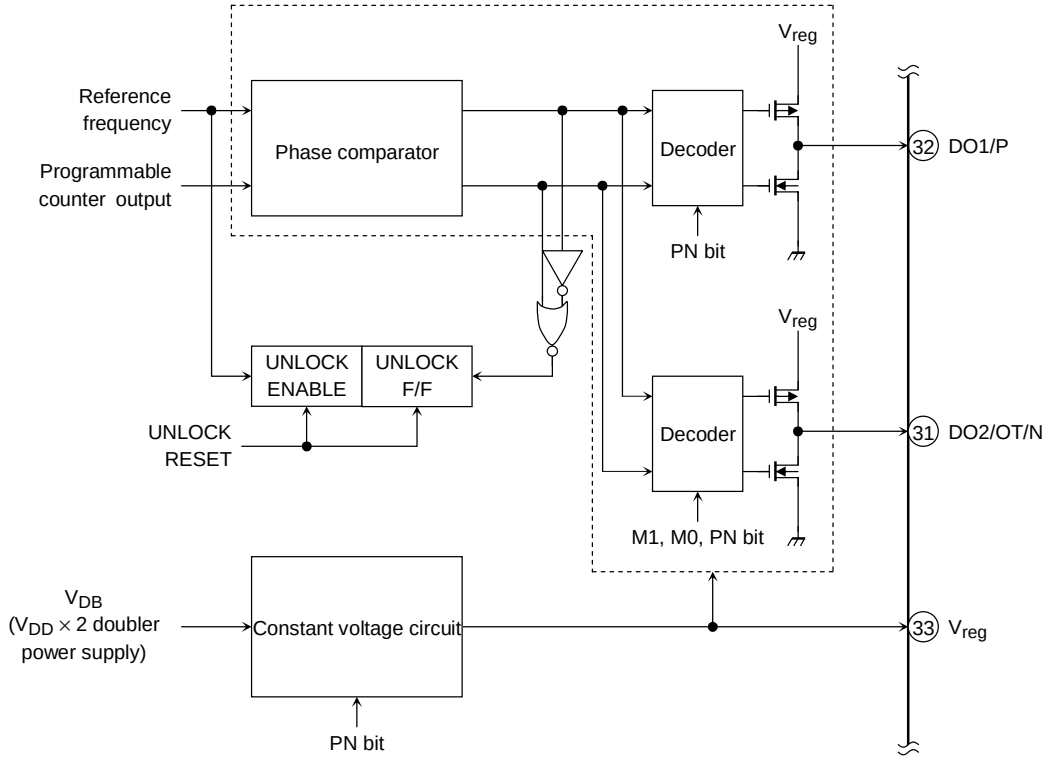
Note: When P/N output and DO output are set up in PLL off-mode state, these outputs are high impedance. This state is held when PLL off-mode or clock stop mode is set up at outputting "L" or "H" level of DO2 pin.

Note: When PN output is setup, "H" level of DO1/2 pin is output as V_{DD} level and V_{reg} potential (1.5 V) is output as "H" level for other settings.

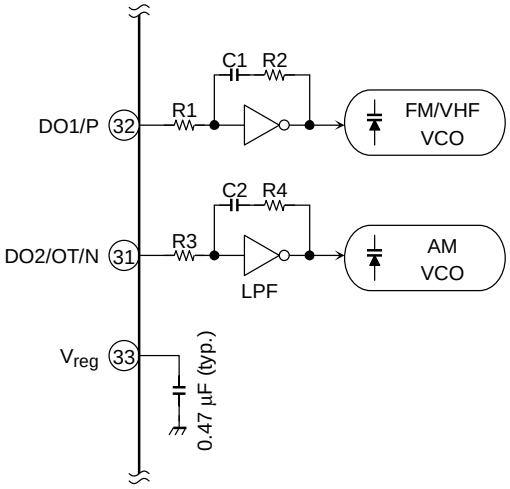
2. Phase Comparator and Unlock Port timing



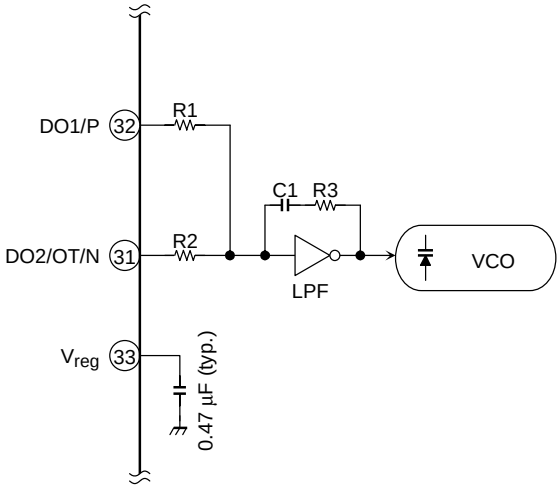
3. Phase Comparator and the Unlock Port Circuit Configuration



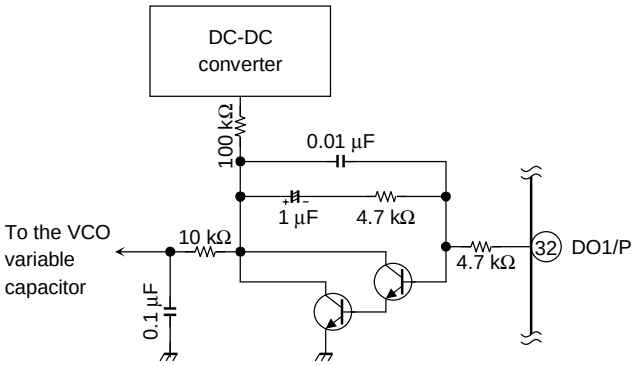
Note: When PLL is off mode and PN bit is set to "1", V_{reg} pin becomes V_{DD} level.



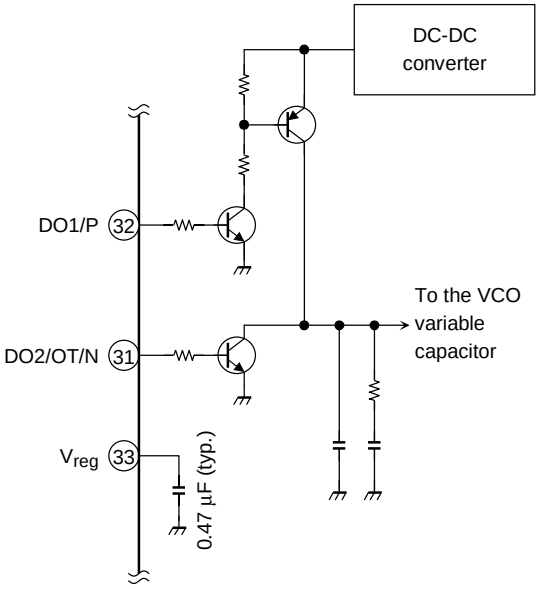
When filter constant is set up for each band



When LPF is used in common (Set DO2 as high impedance and switch the filter constant)



Example of an active low pass filter circuit (for reference)



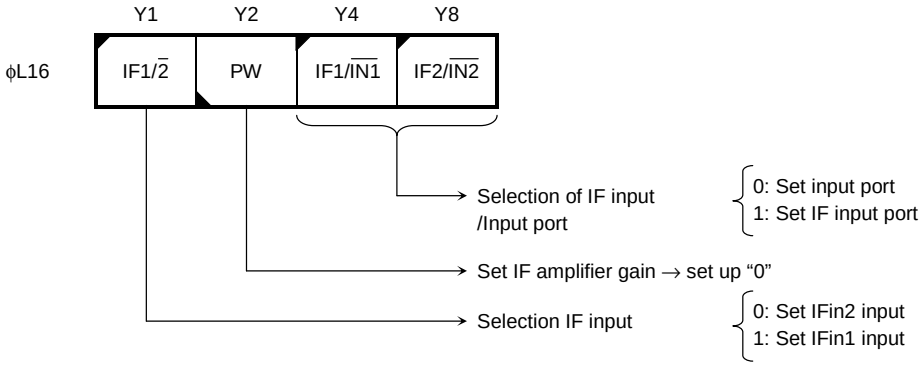
Example of external charge pump circuit (when PN = "1" is set up)

Note: The filter circuits illustrated in the above diagrams are for reference purposes only. It is necessary to examine the system band configuration and characteristic and design actual circuits in accordance with requirements.

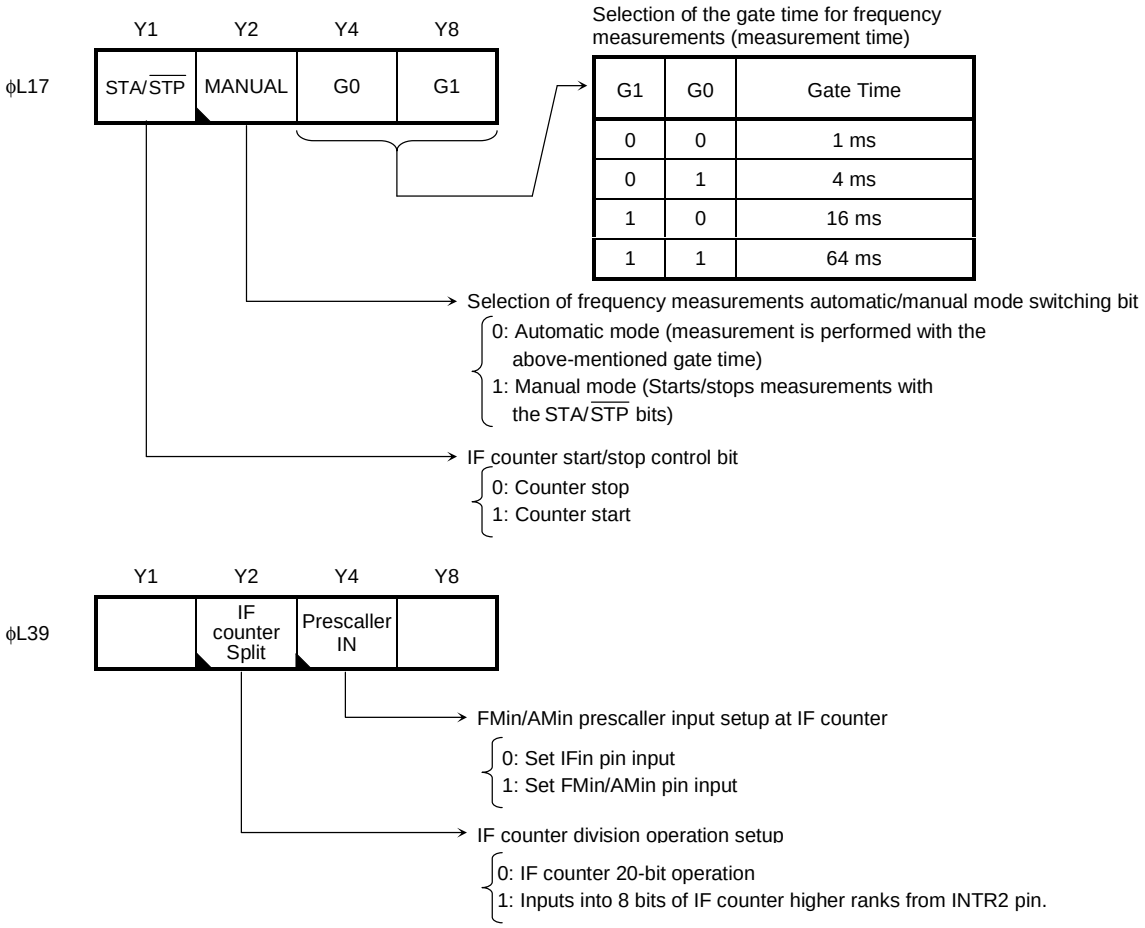
○ IF Counter

The IF counter is 20-bit general-purpose IF counter that calculates FM and AM intermediate frequencies (IF) during auto-tuning and can be used for detecting auto-stop signals, etc. VCO of an analog tuner is measured and detection of received frequency and detection of CR oscillation frequency can be performed.

1. IF Counter Control Port and Data Port

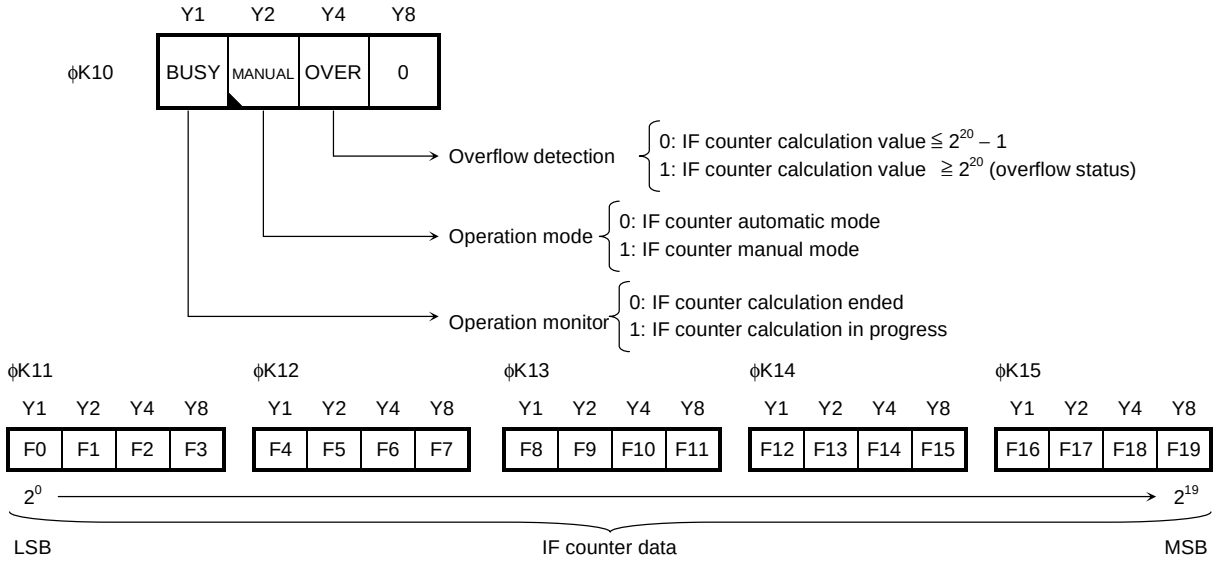


Note: At the time of an input port setup, the pin becomes CMOS input type and be able to detect frequency by IF counter.



Note: When a prescaller input is set as IF counter input, at the time of a setup of a pulse-swallow system, pre-scsler; 1/15•16 are fixed to 16 division, and this frequency is inputted into IF counter.

Note: When a division operation setup of the IF counter is carried out, the counter of 8 bits of higher ranks is inputted from INTR2 pin. However, only 8 bits of this higher rank cannot perform a gate setup by the auto mode. Reset of this counter is reset by setting up "1" to STA/STP bit.



Note: When it is set as IF input, in PLL off-mode, IF input amplifier is turned off in PLL-off mode. In using IF counter in PLL off-mode, it sets it as an input port (CMOS input).

Note: The input amplifier un-chosen by IF1/2 bit. If input amplifier turns off, this input will serve as high impedance.

(1) IF counter automatic mode

A setup in the auto mode of IF counter is set "0" to MANUAL bit and gate time is set up according to the frequency band to measure. If the STA/$\overline{\text{STP}}$ is set "1", operation of IF counter will be started and the set-up clock in gate time will be inputted, and this number of input pulses is counted and it ends. An end of the calculation of IF counter can be judged by referring to BUSY bit. When more 2^{20} pulses are inputted for a total numerical value, OVER bit is set to "1". BUSY bit and OVER bit are judged "0" and the frequency inputted can be measured by taking in IF data of F0-F19.

(2) IF counter manual mode

By internal time base (10 Hz etc.), it is used when gate time is controlled and it measures frequency. The manual mode is set "1" to MANUAL bit. At this time, a gate time setup serves as don't care. In STA/$\overline{\text{STP}}$ bit is set to "1", it starts calculation. In STA/$\overline{\text{STP}}$ bit is set to "0", it will end and calculation will take in data by the binary.

(3) An input setup and division setup of IF counter

Usually, intermediate frequency (IF) Measurement is inputted into IFin1 or IFin2 pin input, and measures this frequency. These pins contain input amplifier and small-size width operation is possible. In addition, the following setup is possible to the input to IF counter, and use it for it according to specification.

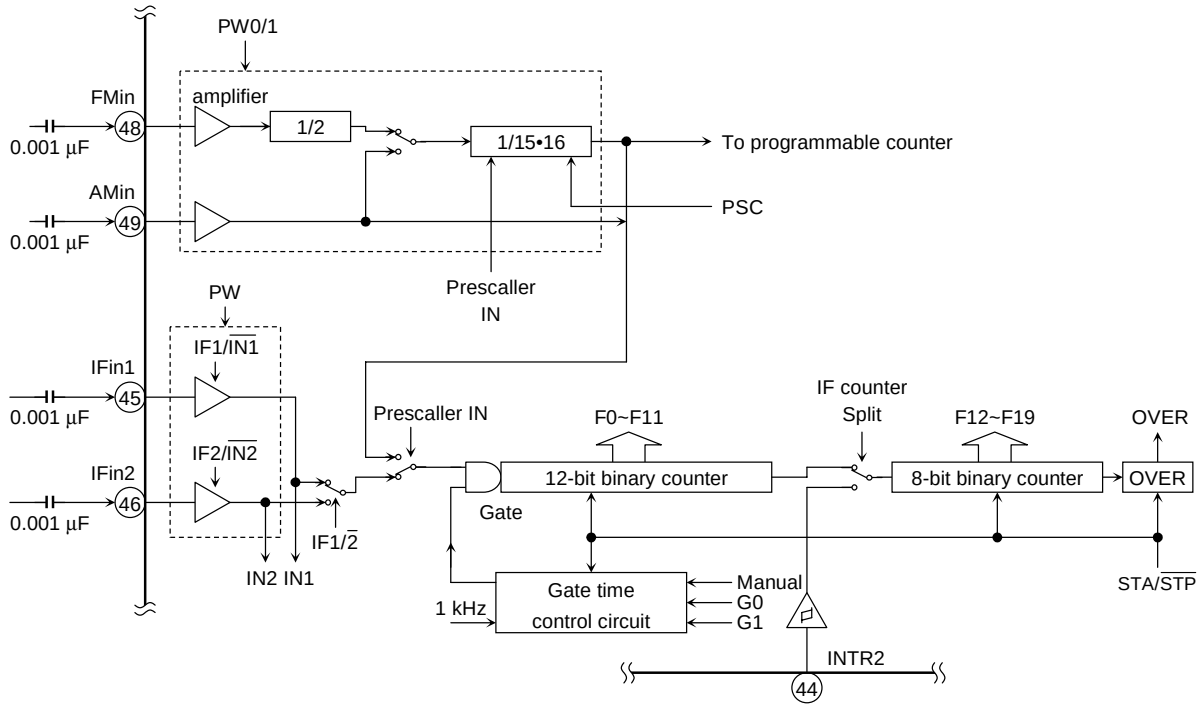
IF1/$\overline{2}$	IF1/$\overline{\text{IN1}}$	IF2/$\overline{\text{IN2}}$	IF counter Split	Prescaller IN	IF Input Setup		
1	0	*	0	0	IFin1 input (Amplifier operation)		
1	1	*	0	0	IN1 (IFin1) input (CMOS input)		
0	*	0	0	0	IFin2 input (Amplifier operation)		
0	*	1	0	0	IN2 (IFin2) input (CMOS input)		
*	*	*	0	1	VHF mode	FMin input (32-divided frequency)	(Note)
					FM mode		
					HF1/2 mode	AMin input (16-divided frequency)	(Note)
					LF mode	AMin input (inputted frequency)	(Note)
*	*	*	1	*	Only 8 bits of higher ranks are inputted from INTR2 pin.		

Note: Refer to the programmable counter item for the input frequency range at the time of prescaller input setup.

2. IF Counter Circuit Configuration

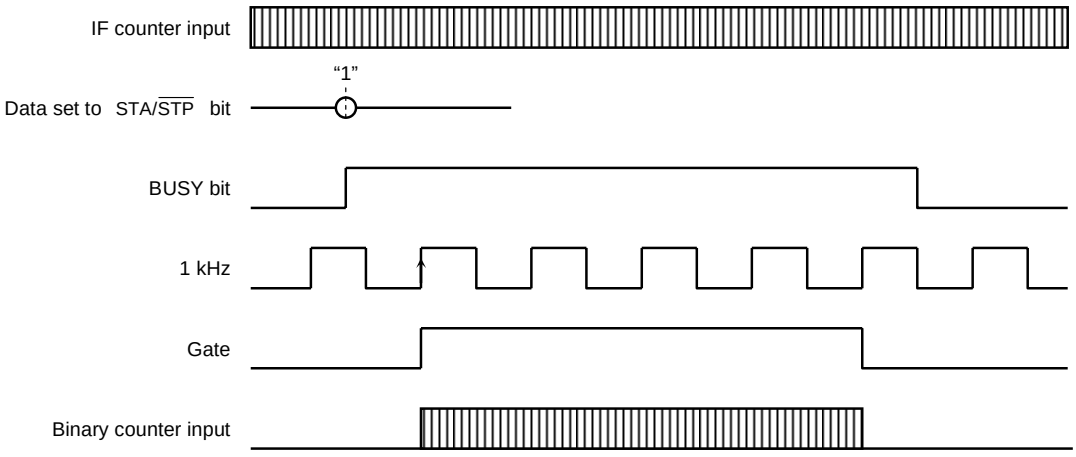
The IF counter consists of the input amplifier, the gate time control circuit and the 12 + 8 bits binary counter.

The clock of FMin/AMin prescaller and can be inputted as an IF counter.



Note: All the binary counters of IF counter operate in a standup.

Note: At inputting IF counter, dividing frequency of prescaller 1/15, 16 is fixed to 1/16. 1/32 for FMin input, and 1/16 or the direct input for AMin are enabled.



The example of IF counter auto mode operation timing

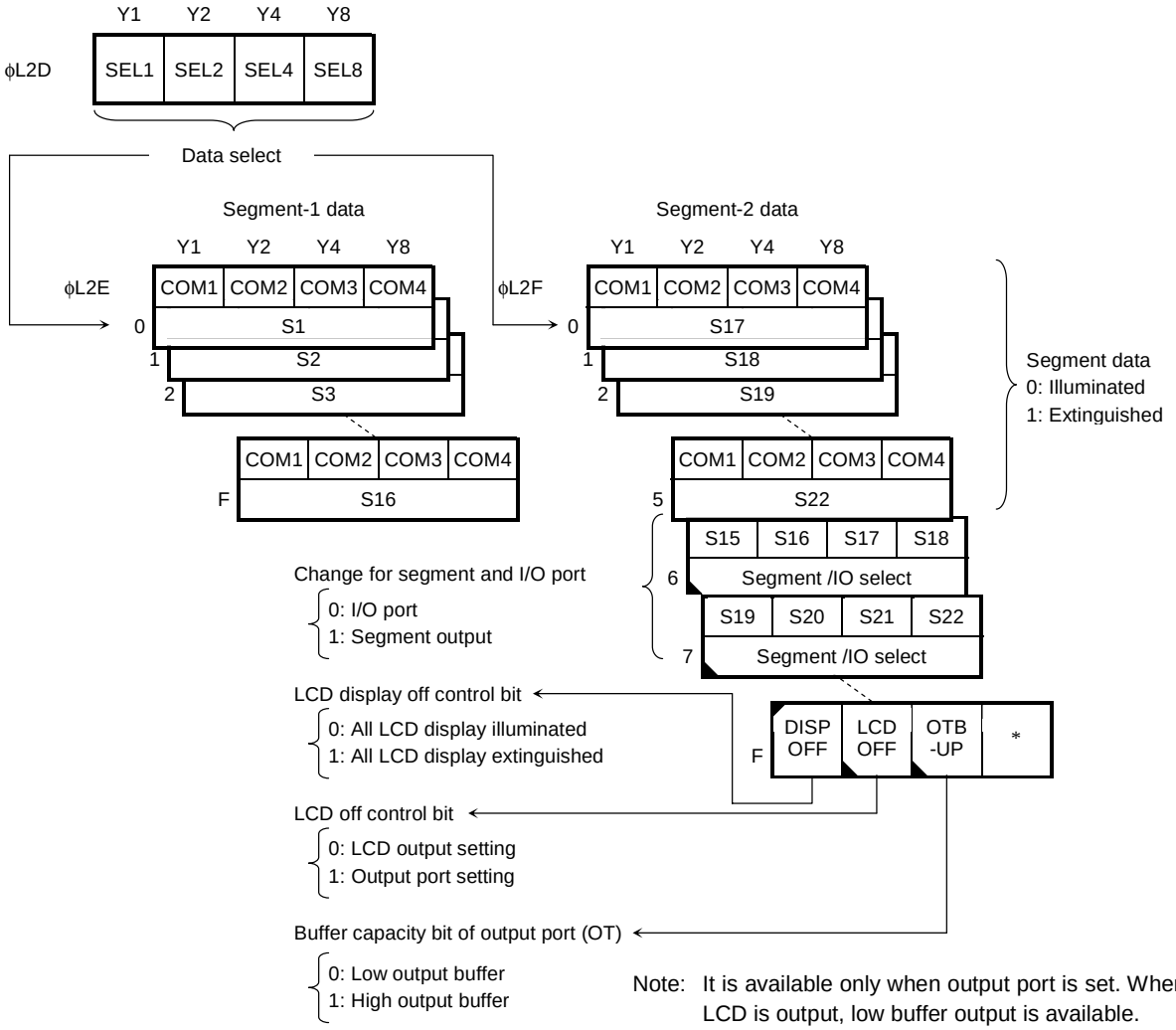
○ LCD Driver

The LCD driver uses the 1/4 duty and 1/2 bias drive method (62.5-Hz frame frequency).

The common output outputs the V_{LCD}, $V_{LCD}/2$ (V_{EE}) and the GND electrical potential, and the segment output outputs the V_{LCD} and GND electrical potential.

A combination of four common outputs and 22 segment outputs enables a maximum of 88 segments to be illuminated. The S15 to S22 pin for LCD driver are also used as the I/O port, after system reset is set as an I/O Port, and can perform a change of an I/O Port and a segment output per 1 bit. All LCD output pins (COM1-S14) can be changed to an output port. The LCD driver is built-in a constant voltage circuit (V_{EE} = 1.5 V) for display purposes and a voltage doubler circuit (V_{LCD} = 3.0 V), The constant voltage circuit for display (V_{EE}) is used as for twice doubler voltage (V_{DB}) is used. For this reason, LCD display stabilized even if power supply voltage was set to 0.9 V is possible.

1. LCD Driver Port



Note: When "1" is set at DISP OFF bit, common output becomes V_{EE} level and all displays are turned off. Different from the situation in which all segment data is set to "0" at display status, the contrast slightly becomes bad. If extinguished status by DISP OFF bit is not favorable, set "0" to DISP OFF bit and all segment data, or set "1" to LCD bit and output "L" level at output port.

Note: Segment data controls lighting/putting out lights of the segment corresponding to a common output and a segment output.

Note: At the time of clock stop mode and about 100 ms after system reset, all the common output and segment output are fixed at "L" level.

The LCD driver control port consists of the segment data selection port and the segment data port. These ports are accessed with OUT2 instruction for which [CN = DH~FH] has been specified in the operand. The segment data for LCD driver is set with the segment data ports (ϕL2E, ϕL2F). The LCD display will be extinguished when the segment data port is set at "0", and will be illuminated when set at "1". Also, the segment-2 data (ϕL2FF) specified with FH in the segment selection port becomes the DISP OFF bit and LCD OFF bit without setting the segment data.

It is possible to extinguish all LCD display with DISP OFF bit without setting the segment data. In this bit, if "1" is set, a common output and non selection wave form (fixed at V_{EE} level) and LCD display all puts out the light. In that time, segment data is held and if DISP OFF bit is set "0", former display is stilled display on LCD. In addition, rewriting of segment data is possible during DISP OFF. Moreover, after reset and CKSTP instruction execution, DISP off-bit is set to "1".

LCD OFF-bit can set all LCD output pins as an output port. In LCD display, this bit is set "0".
(→ Refer to output port item)

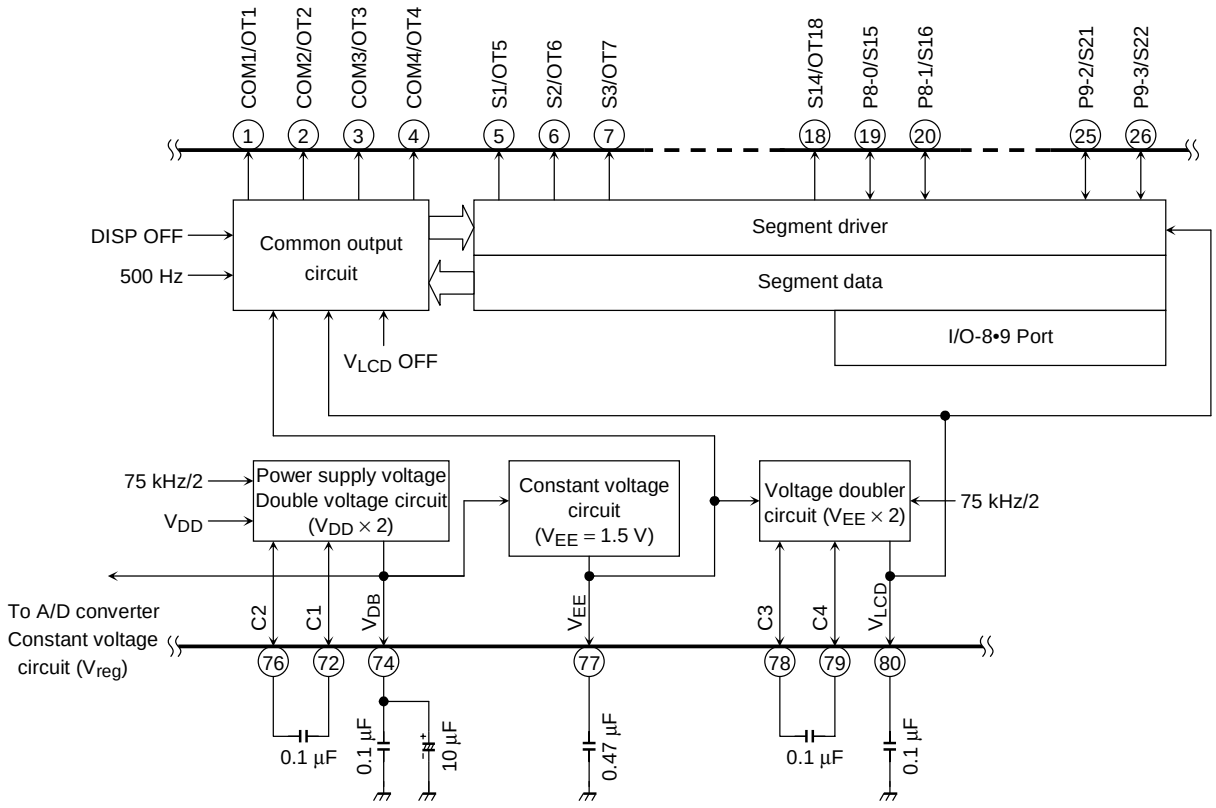
S15 to S22 pin is used as I/O Port. This control is done at segment I/O port select port (ϕL2F6, ϕL2F7).

If the port is set "1", it will become segment output port and set "0", It will become an I/O Port.
(→ Refer to output port item)

These data is divided and undirected setting by data selects port (ϕL2D). Set the data of a specification port of a segment data port in advance and access data port corresponding to it. A data select port is +1 increment whenever accessing data port (ϕL2E, ϕL2F). For this reason, after setting up a data selection port, it can set up continuously.

Note: The data select port is +1 increment automatically by accessing ϕL2E, ϕL2F, ϕL3B, ϕK3B on I/O map.

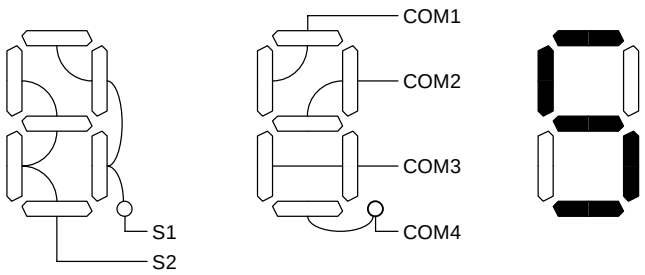
2. LCD Driver Circuit Configuration



Note: In case of setting I/O port, this output port is Nch open drain.

Note: In case of setting segment output as output port in setup "1" to V_{LCD} OFF bit, "H" level of all output becomes V_{LCD} potential output. When "H" output is made into V_{DD} remove the capacitor between C3/C4, and connect V_{LCD} and V_{DD}.

Note: During the clock stop mode and reset, the potential of $V_{LCD}/V_{EE}/V_{DB}$ becomes as V_{DD} level.



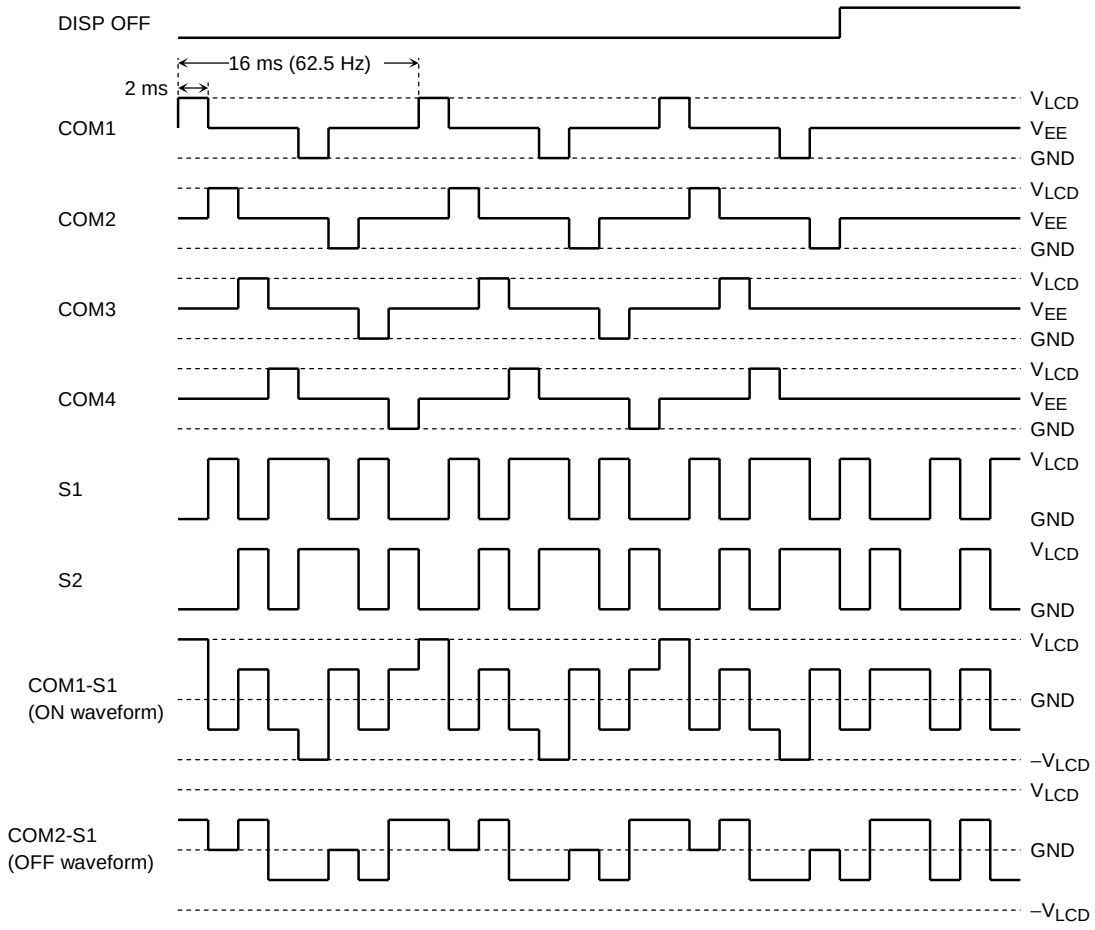
The example of segment data

Segment data -1 (ϕL2E)

	Y1	Y2	Y4	Y8
0	COM1	COM2	COM3	COM4
(S1)	1	0	1	0

	Y1	Y2	Y4	Y8
1	COM1	COM2	COM3	COM4
(S2)	1	1	0	1

Segment data selection (ϕL2D)

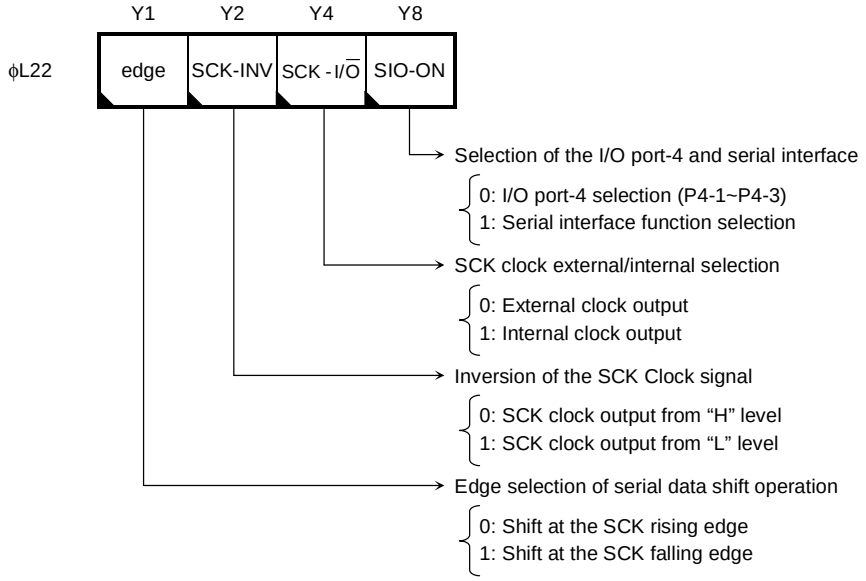


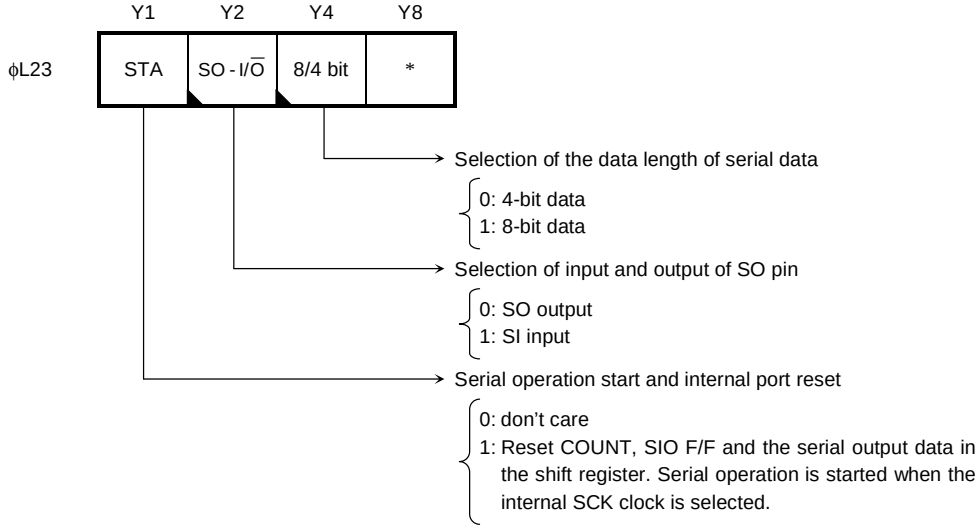
The potential of LCD driver waveform outputs the potential of V_{LCD} and GND, and the middle potential level.

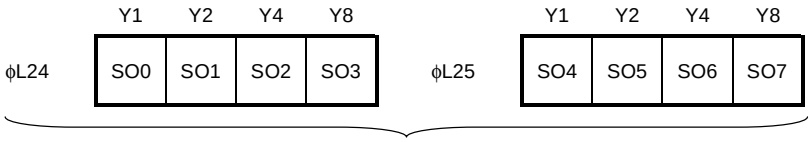
○ Serial Interface

The serial interface is the serial I/O port which transmits and receives 4 bits or 8 bits data synchronizing with the internal or external serial clock. SI, SO and SCK pins perform the transmission and reception with LSI for extension and a microcomputer, etc. When a serial interface operation is finished, interruption is occurred.

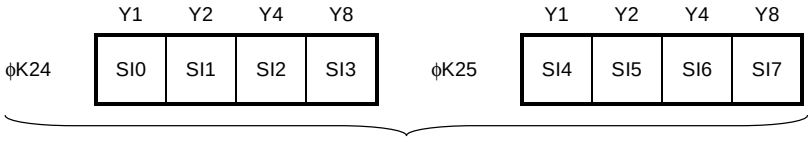
1. The Serial Interface's Control Port and Data Port





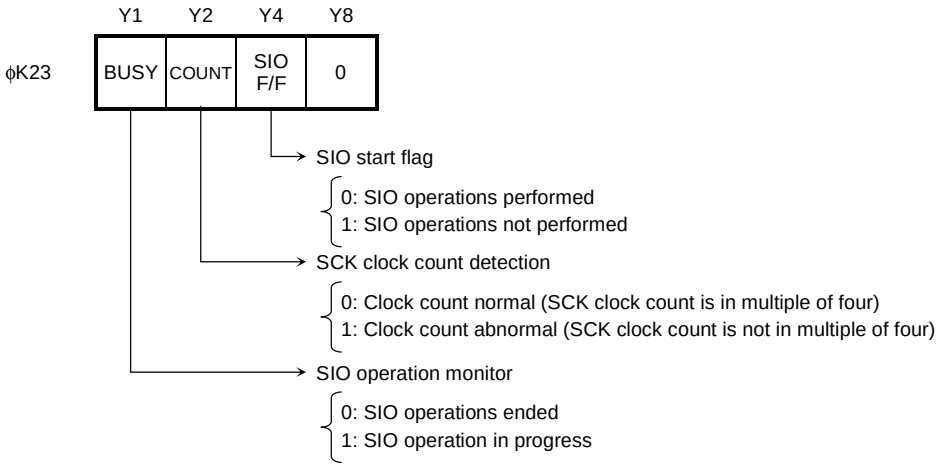


Serial output data: The data set in these ports is output in the serial format



Serial input data: It is possible to load data input in the serial format into data memory

Note: At serial data input, the contents of shift register are accessed as they are.



Serial interface control and data are accessed with the OUT2 an IN2 instruction for which [CN = 2H~5H] has been specified in the operand.

The serial interface pin is used together with the I/O-4 P4-1, P4-2, P4-3 pins, and each of the I/O port-4 pins are switched across to the SI, SO and SCK pins by setting "1" in the SIO ON bit.

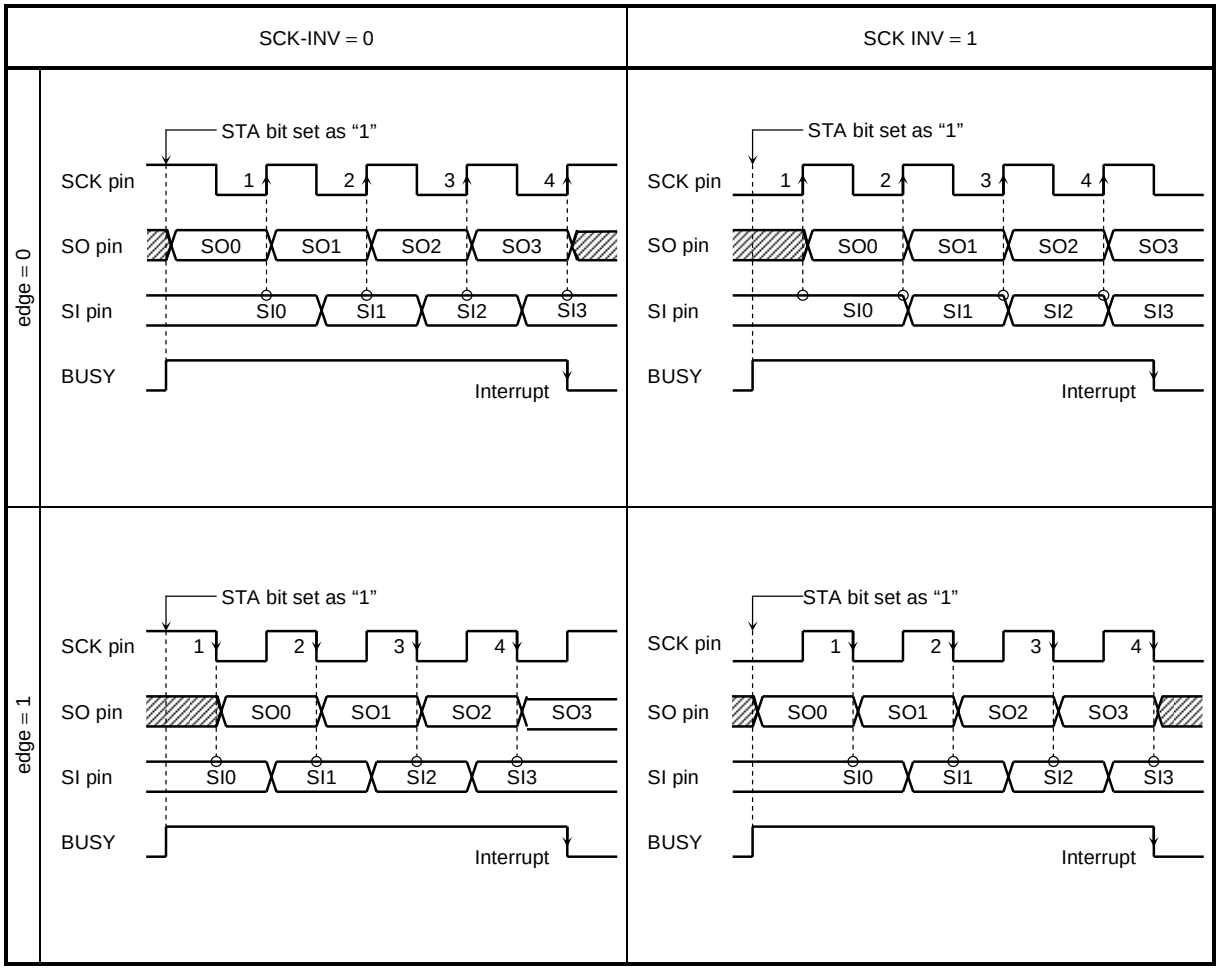
Note: All the inputs of a serial interface build in the Schmidt circuit.

Note: Since SI (P4-1) pin can be used as an I/O Port even when a serial interface is chosen, it can be used for the strike robe signal of SIO etc.
In case of using this pin as a serial input, change into an input state for I/O control bit of P4-1.

(1) edge, SCK-INV, SCK-I/O bit

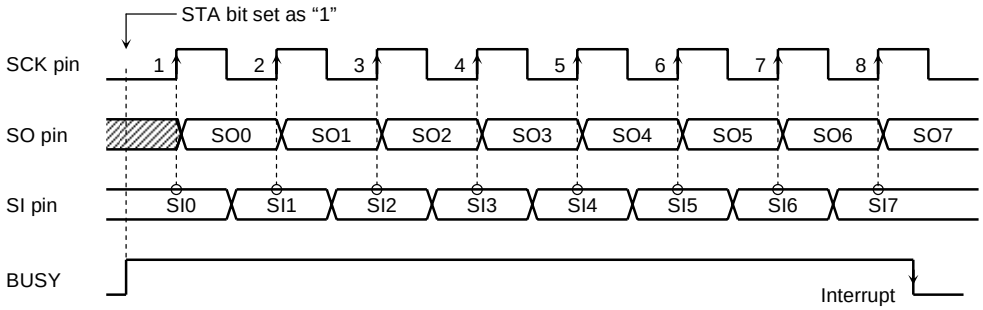
The edge bit setups the edge of a shift and the SCK-INV bit sets up the input-and-output waveform of a shift clock. If the edge bit is set “0”, (SCK) shift operation is done at rising edge and set “1”, (SCK) Shift operation is done at falling edge. SCK-INV bit sets the bit of serial clock output from “H” or L”. In case of setting “0”, it starts shift operation from “H” output, and setting “1”, it starts shift operation from “L” output. These bits perform serial operation as shown in the following table by setup. Set up by the serial format to control.

SCK-I/O bit setups the input-output of serial clock. Usually, when this product is used as a master, set “1” to SCK-I/O bit and then it used as serial clock output and in the case of a slave, set to “0” and then it used as serial input.



(2) 8/4 bit

The 8/4 bit selects the length of the serial data. The length of the serial data is set at 4 bits when this bit is "0", and at 8 bits when this bit is "1". If SIO is started when a serial clock is set as an internal clock, a clock (4 bits or 8 bits) will be continuously outputted by the state of this bit.

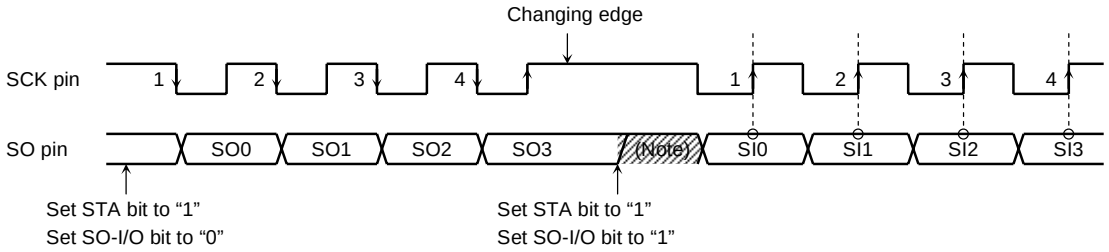


The example of serial operation at the time of setting it as 8 bits

(3) SO-I/$\overline{O}$ bit

The bit sets the serial I/O for the SO pin.

The SO pin outputs serial data when the bit is set at "0", and the SO pin is used for serial data input when this bit is set at "1". This control is used as the serial bus system which outputs and inputs serial data with one pin.



Example for Serial input-output operation

Note: Usually insert pull-up or pull-down in SO pin to prevent floating.

(4) Serial interface operation monitor

The operational status of the serial interface is determined by referring to the BUSY, COUNT, SIO F/F bits.

As the BUSY bit becomes "1" during SIO operations, control data switching and serial data access are performed when the BUSY bit is "0". It interrupts in falling of BUSY bit and a demand is transmitted.

COUNT bit determines if the data sending/receiving has been performed per 4 bits. When shift operation performs with the four multiple, "0" is outputted. When it performs without the four multiple, "1" is outputted.

"1" is set in the SIO F/F bit when the SCK pin starts shift operations.

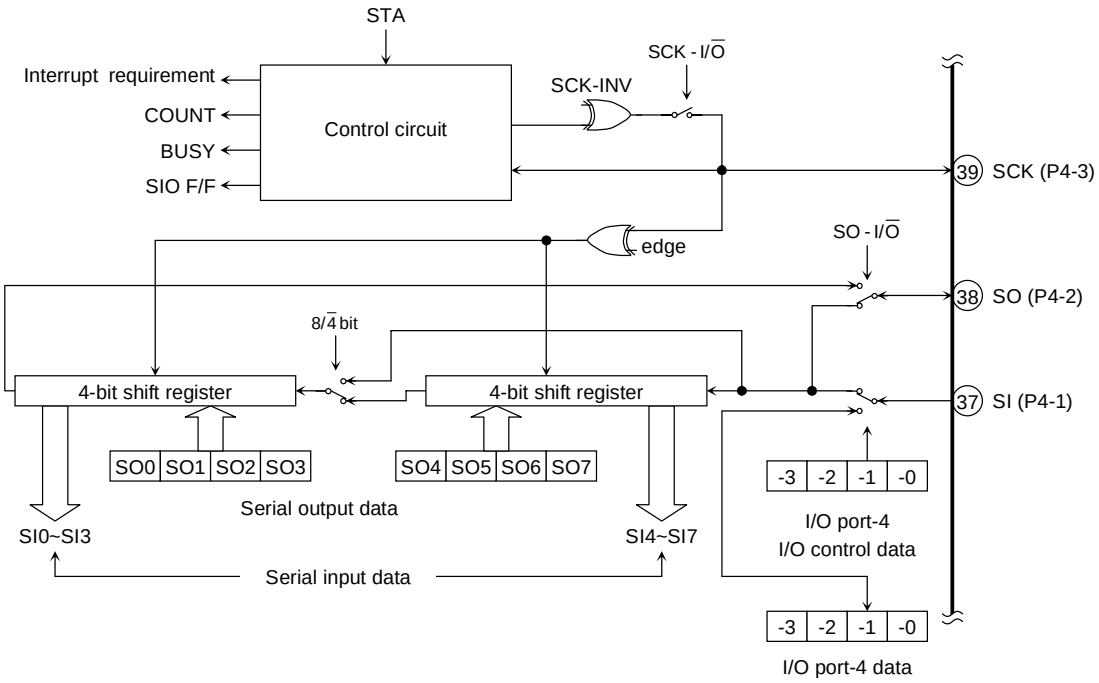
Both COUNT bit and SIO F/F bits are reset to "0" when "1" is set in the STA bit. These two bits are mainly used when the SCK pin sets external clocks (slave mode). An external clock is inputted and it can be judged to be the information that serial data was transmitted and received whether operation was performed normally.

Usually, since interruption is transmitted, interruption processing performs a serial interface end.

(5) STA bit

STA bit is a bit of starting serial interface operation. Serial operation is started whenever STA bit sets “1”. If STA bit setups “1”, serial output data will be transferred to a shift register, and COUNT bit and SIO F/F bit will be reset. When SCK clock is made an internal setup, a serial clock is outputted, and when an external setup of the SCK clock is carried out, it will be in the state waiting for a serial clock input.

2. Configuration of the Serial Interface



The serial interface consists of a control circuit, a shift register, and an I/O Port.

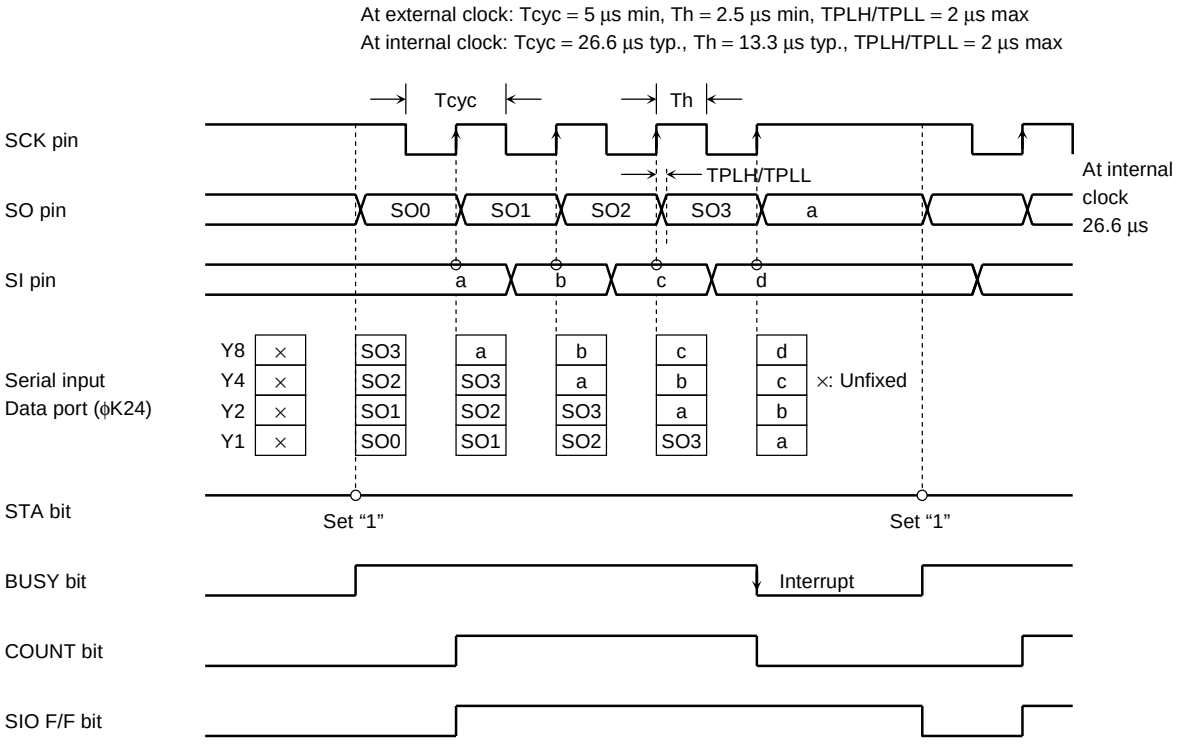
Note: SI pin can be used as I/O Port -4 (P4-1).

Note: As for data and serial input data, the contents of a shift register are taken in by the data memory. For this reason, the contents of the data set to serial output data and serial input data are not in agreement.

Note: All serial input pins are the Schmitt input type.

3. Serial Interface Timing

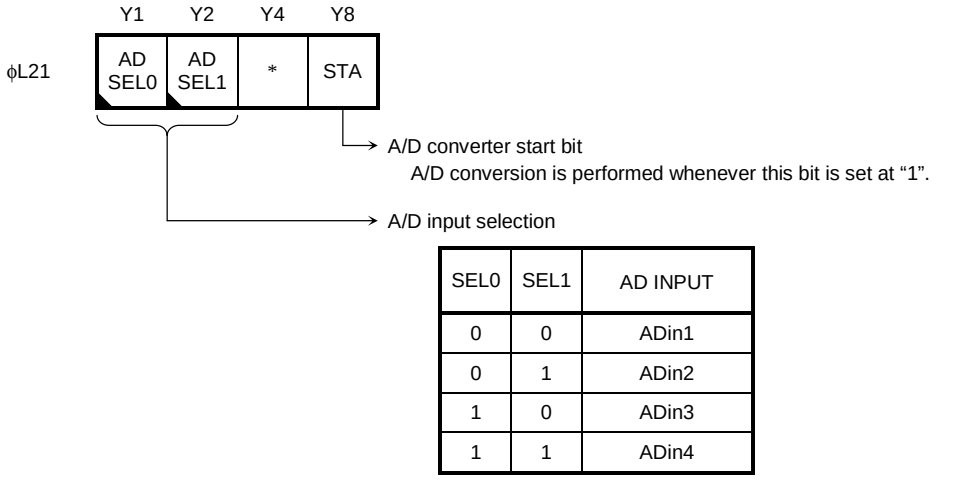
The clock frequency outputted from SCK pin when SCK clock is set as an internal clock is 37.5 kHz (Duty. = 50%). When SCK clock is considered as an external input, the clock of a maximum of 200 kHz can be inputted.



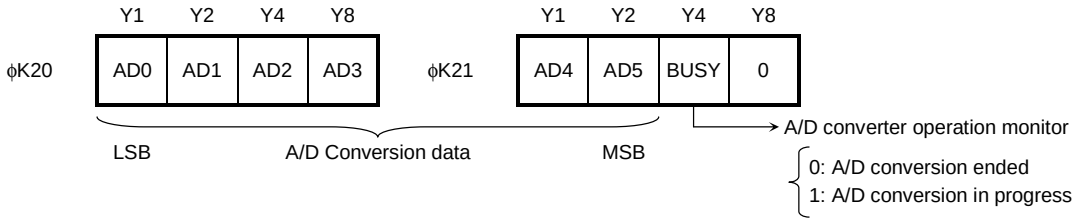
○ A/D Converter

The A/D converter is used for measuring the strength of electric fields and the voltage of batteries with 4-channel 6-bit resolution.

1. A/D Converter Control Port and Data Port



SEL0	SEL1	AD INPUT
0	0	ADin1
0	1	ADin2
1	0	ADin3
1	1	ADin4



A/D converter is the serial comparison systems of 6-bit decomposition ability.

The standard voltage of A/D conversion is an internal power supply (V_{DD}). The voltage which divided this power supply into 64 and A/D input voltage is compared, and data is outputted to A/D conversion data port. A/D conversion input follows multiplex method for the 4-external input pins (ADin1~ADin4 pin), and selected by AD SEL0/1 bit.

The A/D converter performs A/D conversion whenever the STA bit is set at "1", and this is ended after seven machine cycles (280 μs). A/D conversion completion is determined by referring the BUSY bit, and the A/D conversion data is loaded into the data memory after conversion has finished.

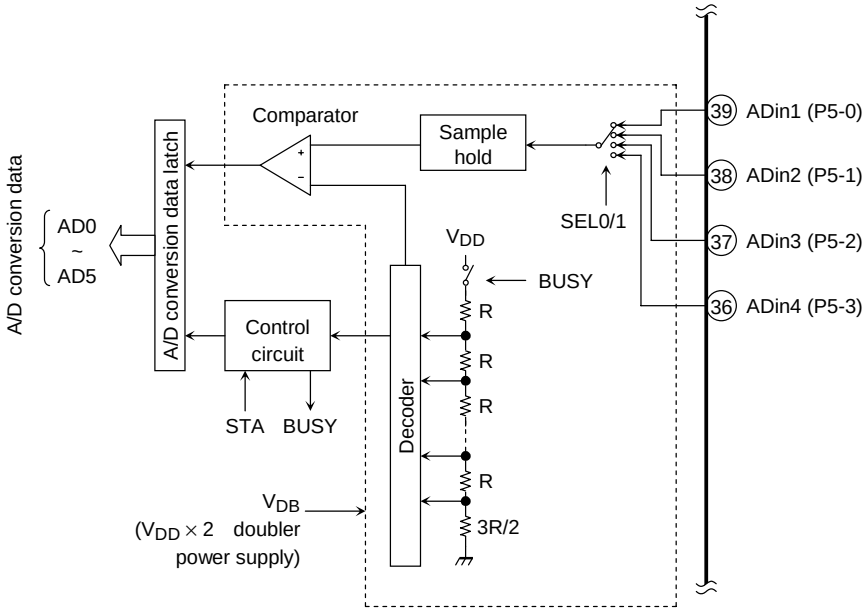
The result of A/D conversion is required for by the following calculation.

$$V_{DD}\times\frac{n-0.5}{64}\ (63 \geqq n \geqq 1) \leqq \text{A/D Input voltage} \leqq V_{DD}\times\frac{n+0.5}{64}\ (62 \geqq n \geqq 0)$$

(n is A/D conversion data value. [decimal])

These control are accessed with the OUT2/IN2 instruction for which [CN = 0H, 1H] has been specified in the operand.

2. A/D Converter Circuit Configuration



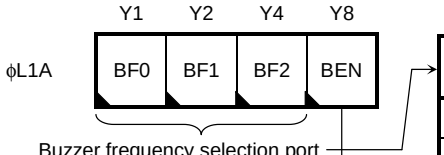
The A/D converter consists of a 6-bit D/A converter, a comparator, an A/D conversion latch and control circuit. Only when BUSY bit is "1", 6 bit D/A converter and a comparator part is in order to operate, there is no current consumption of A/D converter when it is not operating. A/D converter part is driving using by doubler voltage V_{DB} (two times to V_{DD}).

Note: To the output data of I/O Port -5 (Nch open drain) corresponding to A/D input pin to use set up "1" and use it by changing into an input state.

○ Buzzer Output

The buzzer output can be used to output tones and alarm tones to confirm key operations and the tuning scan mode. Buzzer type can be selected from a combination of four output modes and eight different frequencies.

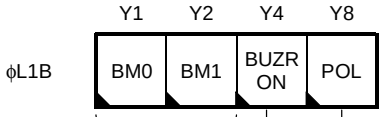
1. Buzzer Control Port



BF2	BF1	BF0	Buzzer Frequency	Duty
0	0	0	0.625 kHz	1/2
0	0	1	0.75 kHz	1/2
0	1	0	1 kHz	2/3
0	1	1	1.25 kHz	1/2
1	0	0	1.5 kHz	1/2
1	0	1	2.08 kHz	2/3
1	1	0	2.5 kHz	1/2
1	1	1	3 kHz	2/3

Buzzer output enable bit

0: Buzzer output fixed (at POL = "0", "L" level, at POL = "1", "H" level)
1: Buzzer output enabled



Buzzer output logic setup

0: Positive logic output. Buzzer frequency is outputted in positive logic from "L" level
1: Negative logic output. Buzzer output is outputted in negative logic from "H" level

P4-0 of I/O port-4 and buzzer output selection

0: I/O port-4 (P4-0) selection
1: Buzzer output selection

BM1	BM0	Buzzer Output Mode	
0	0	Continual output	(mode A)
0	1	Staggered output	(mode B)
1	0	10-Hz intermittent output	(mode C)
1	1	10-Hz intermittent output with 1Hz intervals	(mode D)

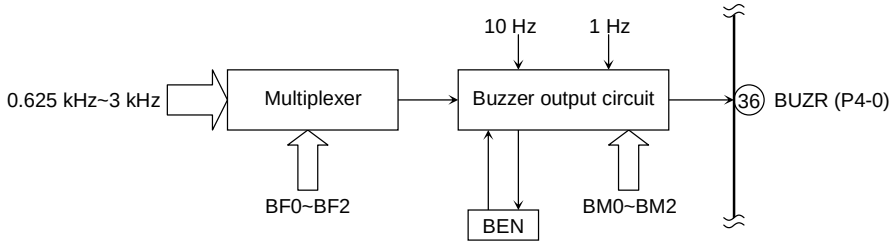
The buzzer output is also used P4-0 I/O Port. In order to set it as a buzzer output, BUZR ON bit is set to "1" and it changes to a buzzer output by setting it as an output by the P4-0 I/O control port. After logic setting up of buzzer frequency, mode setup and a logic setup, buzzer enable bit is set to "1", it outputs buzzer. At the time of condition setup, buzzer enable bit is setup "0".

In Continuation output mode (mode A), if buzzer enable bit is set "1", buzzer frequency will be outputted continuously, and if "0" is set, a buzzer output will stop. In staggered output mode, whenever buzzer enable bit is set to "1", buzzer is outputted for 50 ms and stopped. In this mode, when "1" is reset to the buzzer enable bit during buzzer output (50 ms), 50 ms is extended and the buzzer of 100 ms can be outputted. If it is reset during the extra 50 ms, 150 ms is extended and the buzzer output time can be easily set up. If 10 Hz intermittence output mode (mode C) sets "1" to the buzzer enable bit, 50-ms buzzer output and 50-ms buzzer pause are performed continuously. And a set of "0" stops a buzzer output.

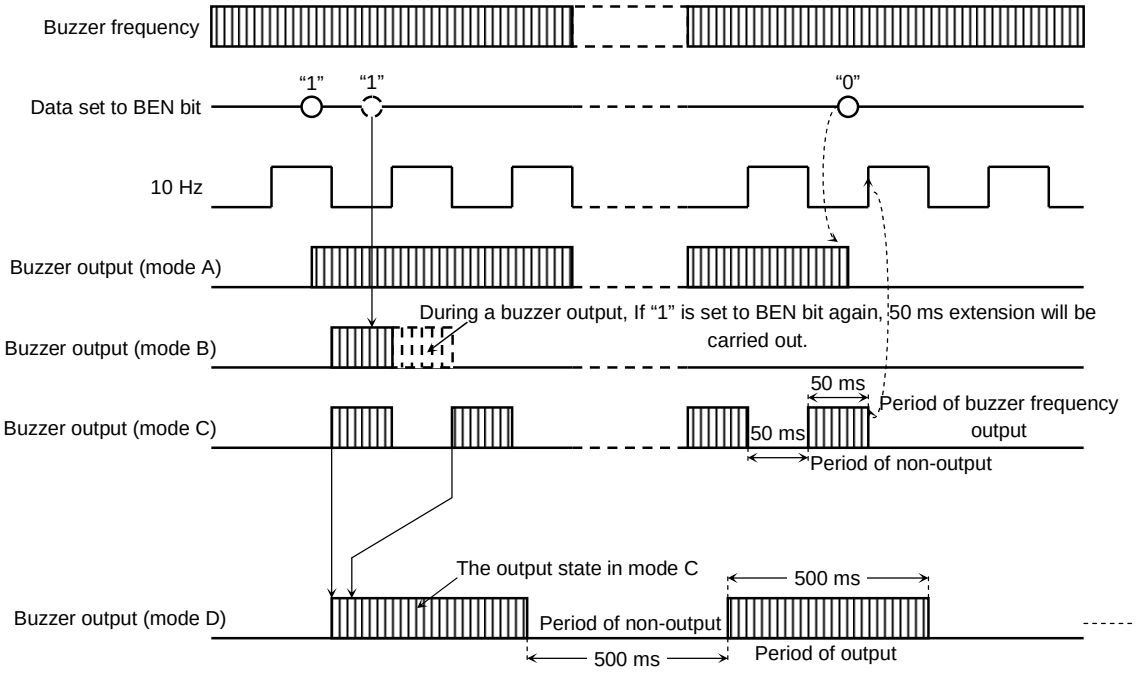
10-Hz intermittent output with 1 Hz intervals mode (mode D), if buzzer enable bit is set "1", 50-ms buzzer output and 50-ms buzzer pause will carry out 500-ms output, after that 500-ms pause output of 50-ms buzzer output and the 50-ms buzzer pause is carried out again, and this operation is repeated. A set of "0" stops a buzzer output. At mode B, C, and D, a buzzer is in an output state, even if it sets "0" to buzzer enable bit and it makes it stop, the buzzer of 50 ms is outputted and stops. In addition, a buzzer output state can be judged according to the contents of a timer port. The timer port 10-Hz bit is "0", buzzer is an output state and it is in a pause state at the time of "1".

The control of buzzer is accessed by the OUT 1 instruction for which [CN = AH, BH] has been specified in the operand.

2. Buzzer Circuit Configuration



3. Buzzer Output Timing

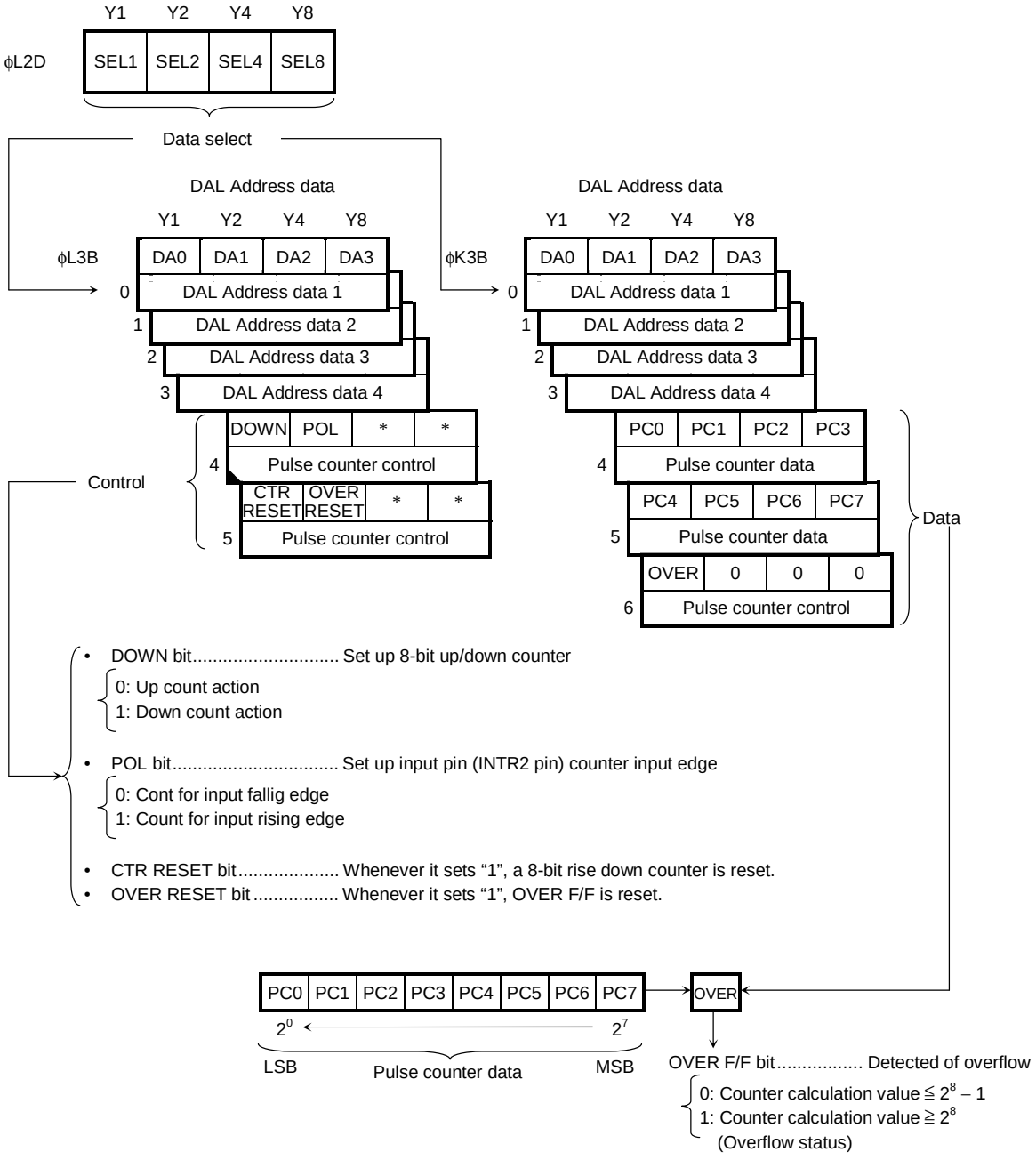


Note: When making a buzzer output, it sets up an output state about P4-0 (set "1" to I/O control port)

○ Pulse Counter

The pulse counter is 8-bit up/down counter and the number of clocks can be detected with CMOS input from INTR2 pin. It can be used for counting and detecting tape run.

1. Pulse Counter Control Port, Data Port



The pulse counter measures pulse number of INTR2 pin.

POL bit set up the clock edge of input pin. If "0" is set, it will count in the falling of an input and it will set to "1", it will count in the rising of an input. Usually, this bit is used fixed.

DOWN bit sets up a up/down of 8-bit counter. If it sets to "0" and it will set to rise count operation and "1", down count operation will be done. A change of a up/down can be performed freely. However, if a clock pulse is inputted during change command execution, since it is canceled, be careful of this count.

When 2^8 or more pulses are inputted, OVER F/F bit is set to "1". When performing count operation of 8-bits or more, this OVER F/F are detected, and on a data memory, only the number of times of overflow is added and subtracted, and can correspond. After detection by this bit, and OVER RESET bit is set "1" and OVER F/F is reset.CTR RESET bit resets only 8-bit counter. The counter is reset whenever it sets "1".

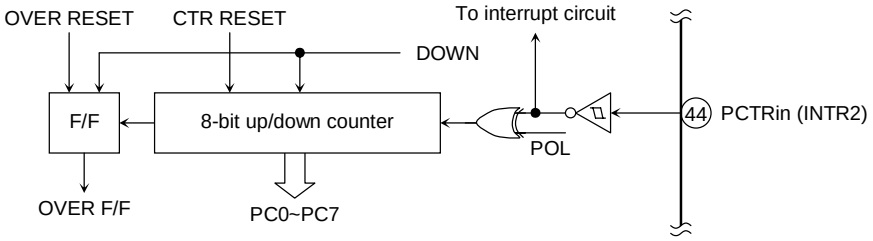
Counter data loaded data in a data memory by the binary.

The control of pulse counter and data loading is accessed with the OUT3/IN3 instructions for which [CN = BH] have been specified in the operand and arranges in DAL address register port. This port is set up by data select port (ϕL2D), which specified the division. The data of a specification port is set beforehand and the data port corresponding to it can be accessed. The data select port is +1 increments whenever it accesses DAL address port (ϕL3B, ϕK3B). For this reason, after setting up a data selection port, it can set up continuously.

Note: If POL bit is changed, a clock pulse may enter. Reset data by the reset bit after changing.

Note: If data select port is +1 increments when it accesses ϕL2E, ϕL2F, ϕL3B, ϕK3B on the I/O map.

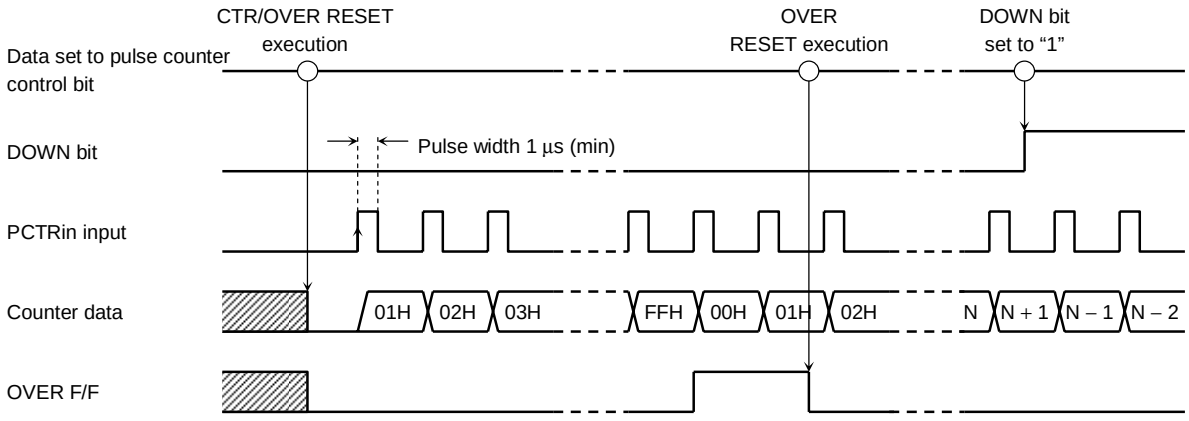
2. Pulse Counter Circuit Configuration



Note: Pulse input is the Schmitt input type.

Note: It can be used as pulse counter and interrupt function (INTR2 pin input) together.

3. Example for Pulse Counter Timing

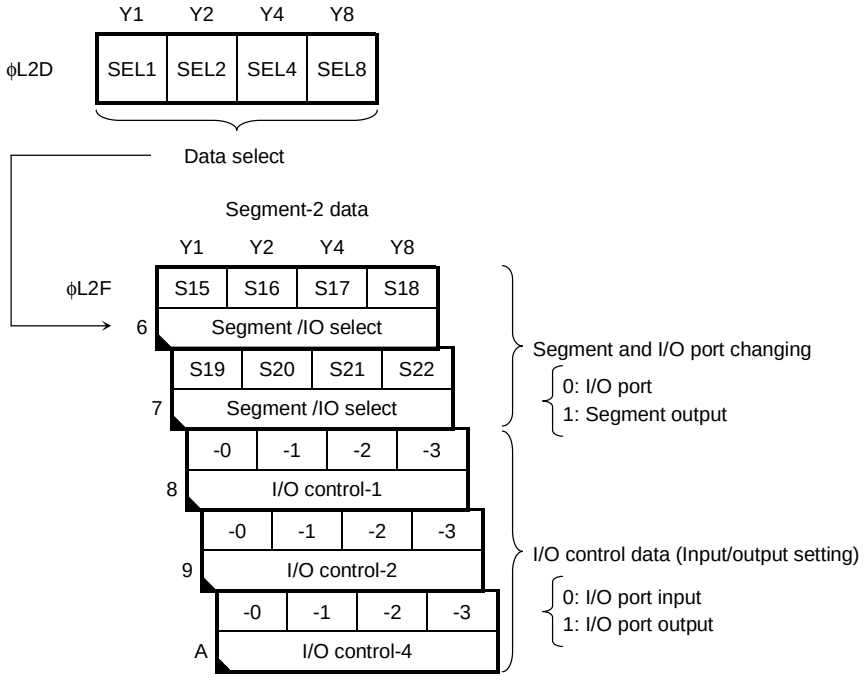


○ Input and Output Port (I/O Port)

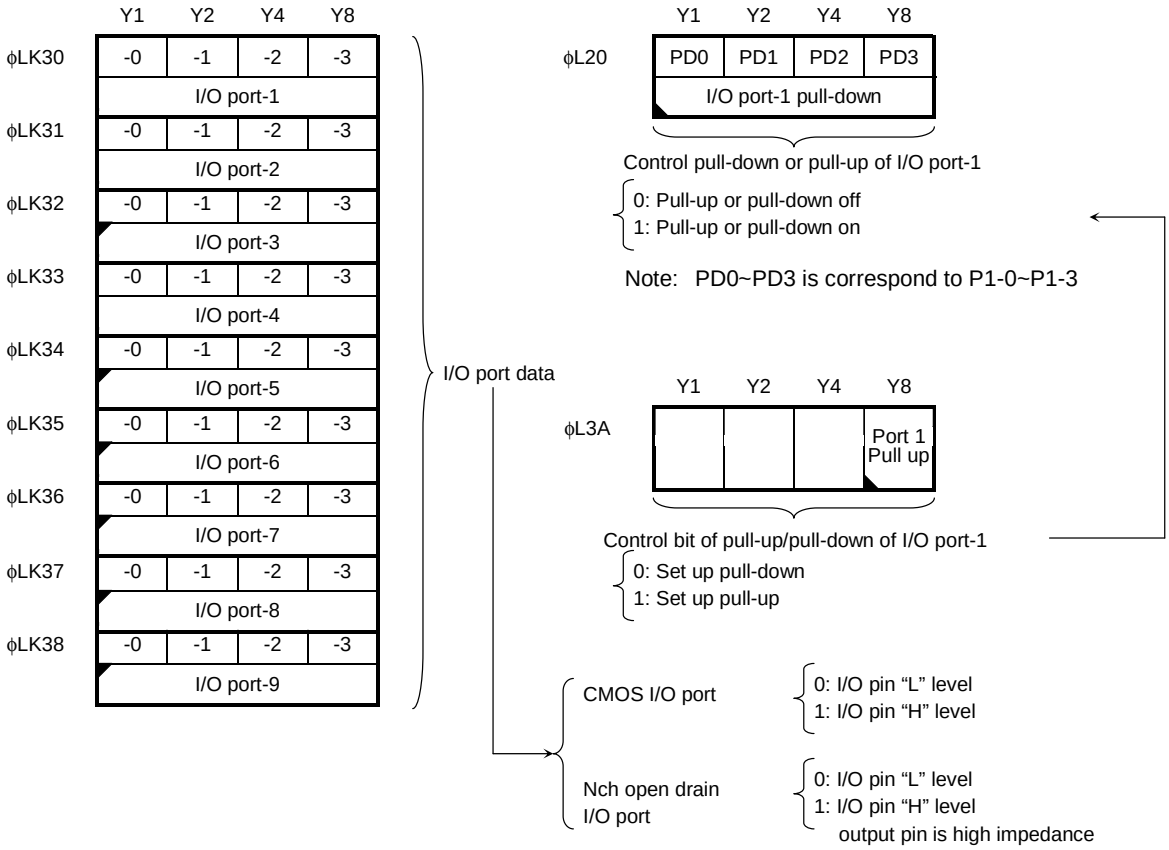
There are 36 I/O ports available between I/O port-1~-9 which are used to input and output control signals. Of these 36 I/O ports, 12 I/O ports are CMOS type and 24 I/O ports are Nch open drain type. The combination function and the functional feature of each I/O port are as follows.

I/O Port		Combination and Additional Function	Structure
I/O port-1		It's possible to set pull-up/pull-down. But, mixture of a pull-up pull down is impossible.	CMOS
I/O port-2	P2-0~-2	—	
	P2-3	Pre-scaller PSC output	
I/O port-3		Nch high output buffer Output withstand voltage 3.6 V (max)	Nch open drain
I/O port-4	P4-0	Buzzer output	CMOS
	P4-1~3	Serial interface input/output port	
I/O port-5		6-bit A/D converter analog input The potential to V_{DB} ($V_{DD} \times 2$) can be inputted.	Nch open drain
I/O port-6		Output withstand voltage 3.6 V (max)	
I/O port-7			
I/O port-8		The potential to V_{LCD} (3 V) can be inputted.	
I/O port-9			

1. I/O Port Control, I/O Port Data



Note: I/O-1, I/O-2, - - - - - is correspond to the pin name of P1-0~-3, P2-0~-3, - - - - - .



The I/O port for the I/O ports is set with the contents of the I/O control data port. "0" is set in the I/O control data port bit which corresponds to the relevant port when setting the input port, and "1" is set when setting the output port.

I/O control data port is arranged segment-2 data port and set up by data select port (φL2D), which specified the division. The data of a specification port to set beforehand is set and the data port corresponding to it can be accessed. The data select port is +1 increments whenever it accesses DAL address port (φL2F). For this reason, after setting up a data selection port, it can set up continuously.

The output status of the I/O port is controlled by executing the OUT3 instruction for which corresponds to each I/O port during output port setting. The contents of the data currently output can also be loaded into the data memory by executing the IN3 instruction. In addition, the data read by the IN3 command is not surely in agreement with the data outputted by the OUT3 instruction and, in order to read the state of a pin.

The data input in the I/O port is loaded into the data memory by executing the IN3 instruction for which corresponds to each I/O port during input port setting. The contents of the output latch will have no effect on the input data at this point.

Nch open drain I/O ports have not I/O control data. When it makes an input, it is set "1" in I/O data port, the status becomes high impedance and read the input status into data memory by IN3 instruction. When output state becomes "L" level, it set "0" in I/O data port by OUT3 command.

The execution of the WAIT instruction and CKSTP instruction is cancelled and CPU operations are re-started when the status of the I/O port input specified in the input port changes with I/O port-1. Also, the MUTE port and MUTE bit are forcibly set to "1" during changes in the input status when the MUTE port's I/O bit is set at "1". By control port of I/O port-1 pull-down, it sets up pull-down or pull-up status. It can set up a pull-down or pull-up for every pin and if the port is set up "1", it will become a pull-up or a pull-down. The pull-up/pull-down control bit of I/O Port -1 perform a change of a pull-up and a pull down.

If the bit is set up"0", the status becomes pull-down and set up "1", it becomes pull-up.

Set up the pull-up and pull-down is used for key matrix configuration. I/O Port-1 with a pull down or a pull-up is considered for a usual I/O Port output as an input as an output of a key matrix, and a key matrix is configured. It is able to configure the key matrix of a low noise by the following methods. In setting pull-down to I/O port-1, the output side of a key matrix is usually high impedance (input state), output and scan to "H" level on key loaded line, detected key input or non by loading input status of I/O port-1. In the case of a pull-up, "L" level is outputted and it detected on a key loading line. During executing of CKSTP instruction and WAIT instruction, the existence of this key input can also be judged and restarted. When restarting at the time of CKSTP command execution, I/O Port-1 is used by changing into a pull-up state. For the clock stop mode, since the outputs of an I/O Port are outputted all "L" level, I/O Port-1 stands by in the state of a pull-up, and if a key is inputted, I/O Port-1 input will change and restart. In this case, since the standby time of about 100 ms occurs as time lag after being canceled of a clock stop. Since release of WAIT instruction holds the output state, restarting is possible by the method of both a pull-up and a pull down, and since there is no time lag from release, detection and operation of a key are quickly possible. Using these backup modes together can reduce consumption current.

Since the input of I/O Port-1 is an inverter input, the usage that serves as middle potential cannot be done to this input. But, only at the time of execution of the input instruction, since an input will be in an ON state, even if middle potential is inputted, as for other I/O Port inputs, unusual consumption current does not occur. For this reason, use of the pull-up in potential lower than V_{DD} potential, the three value output of an output level, etc. is possible.

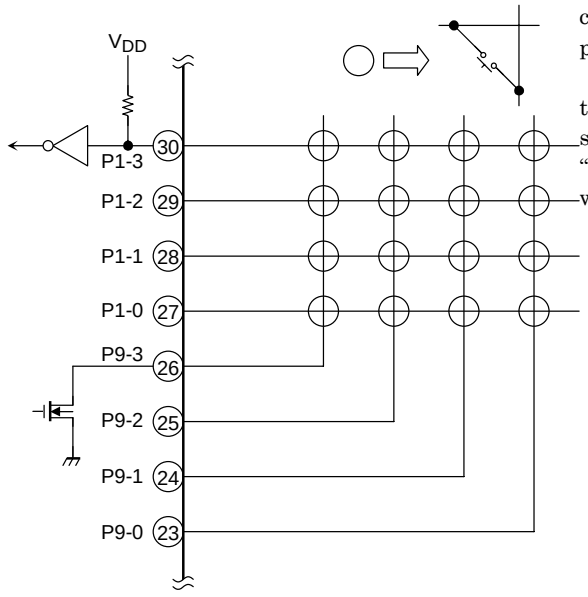
I/O Port -2, -4 pins are the I/O Ports of CMOS structure, P2-3 pin is the prescaller PSC output, P4-0 pin is the buzzer output and P4-1-3 pins are the serial interface serve a double purpose, respectively. I/O port-3, -5~-9 are Nch open drain I/O port.

I/O Port -3 uses V_{LCD} (3 V) for the gate potential of Nch output buffer. For this reason, the output current by which power supply voltage was stabilized also in the time of low voltage can be obtained. This port can perform the input and output to 3.6 V.

I/O port-5 is used as 6-bit A/D converter input. This port is able to inputted V_{DB} potential (the potential to $V_{DD} \times 2$).

I/O Port -8, -9 are also used as LCD driver. V_{LCD} (3 V) is used for the gate potential of an Nch open output buffer. For this reason, the output current by which power supply voltage was stabilized also in the time of low voltage can be obtained. These pins can perform the input and output to V_{LCD} (3 V). These pins are set as the input of an I/O Port after reset.

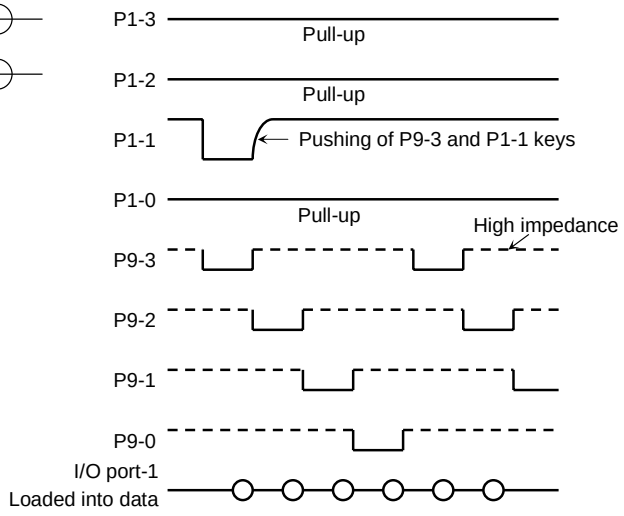
Note: The data select port is +1 increments automatically when it accesses ϕL2E, ϕL2F, ϕL3B, ϕK3B on the I/Omap.



Example for key input matrix circuit configuration

The following is an example of key input matrix circuit configuration. Without key input, it pulled-up and key is pushed, it inputted "L" level from sauce side(I/O port-9).

It is necessary to take into consideration the shift time to the pull-up of a key input from "L". They are all about a key sauce side at the time of WAIT instruction execution and "L" WAIT instruction can be lifted, whenever a key input will be pushed, if it stands by on the level.



○ Register Port

The G-register and data register outlined in the explanation on the CPU are also used as a single internal port.

1. G-register (ϕKL1D, ϕKL1E)

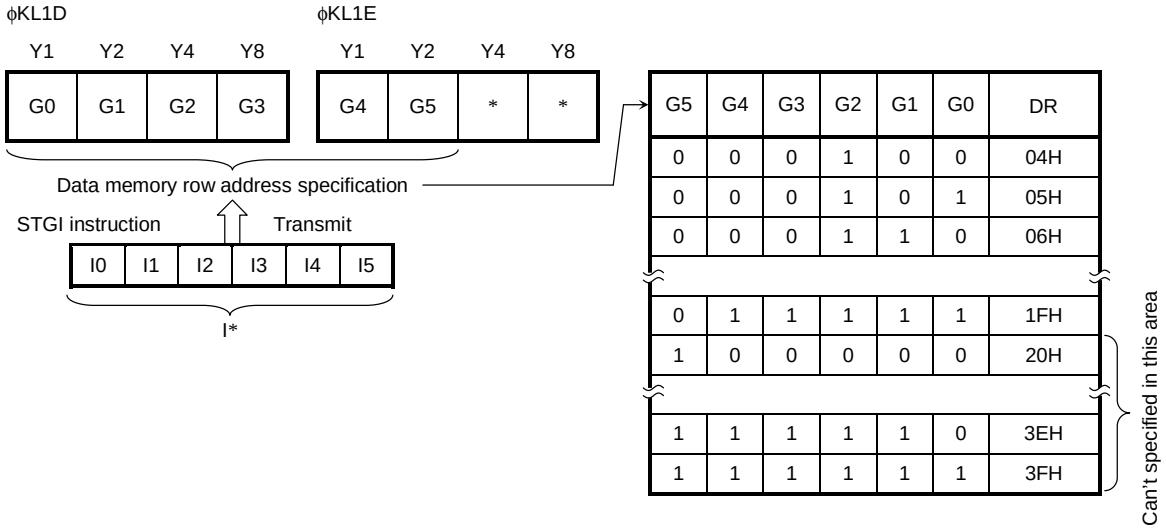
This register addresses the data memory's row addresses (DR = 04H~3FH) during execution of the MVGD instruction and MVGS instruction. This register is accessed with the OUT1/IN1 instruction for which [CN = DH~EH] has been specified in the operand. Moreover, if STGI instruction is used, data can be set to this register by one instruction.

Note: The contents of this register are only valid when the MVGD instruction and MVGS instruction are executed and are ineffective when any other instruction is executed. Moreover, it does not have the influence on this register by MVGD instruction and MVGS instruction.

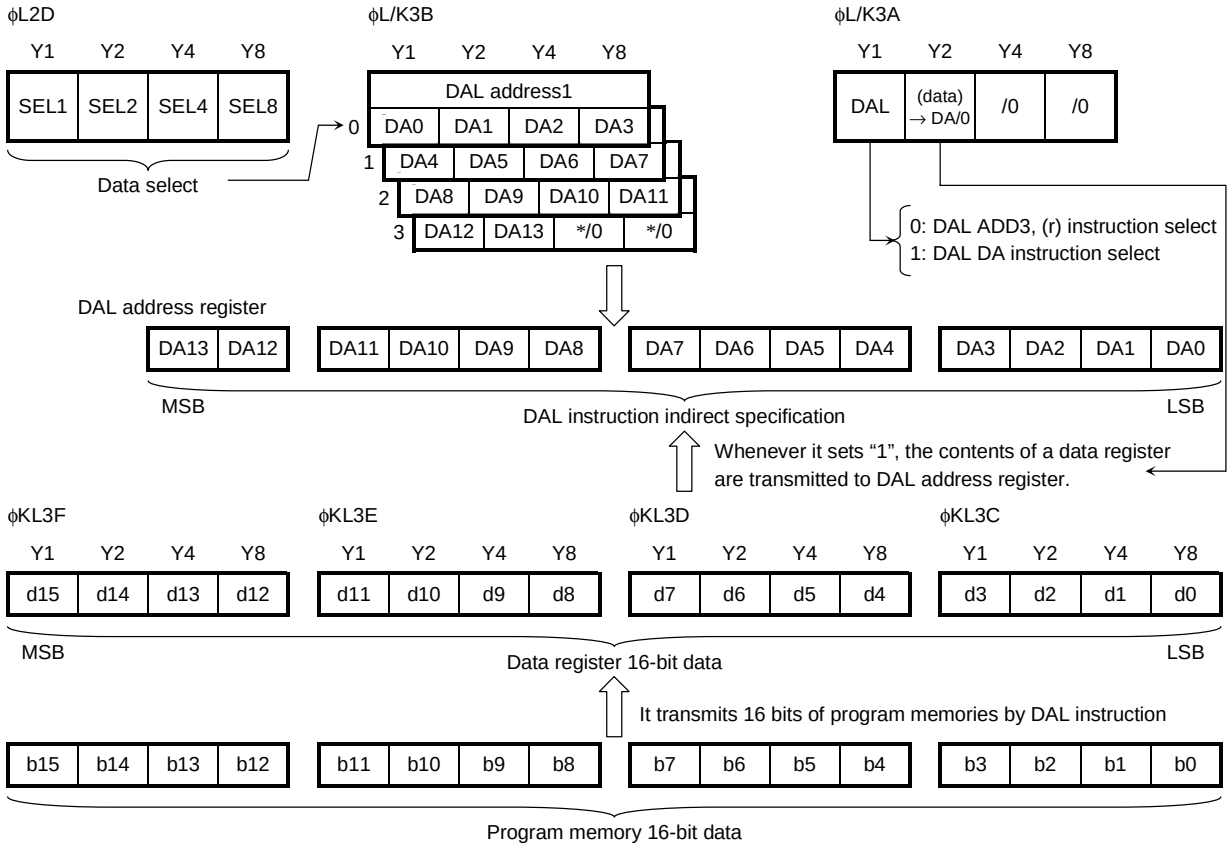
Note: All of the data memory row addresses can be specified indirectly by setting data 00H to 3FH in the G-register. (DR = 00H~3FH)

Note: For a reason with a RAM capacity of 512 words, this product will become unfixed if 20H-3FH is specified to be G-register.

Note: Writing and read-out are possible for this register. Please evacuate and return in a data memory if needed at the time of interruption.



2. Data Register (φKL3C~φKL3F), DAL Address Register (φKL3B0~φKL3B3) and Control Bit



The data register is 16-bit register for which load the program memory data when the DAL instruction is executed. The contents of this register are loaded into the data memory in 4-bit units with the execution of the OUT1/IN1 instructions for which [CN = CH~FH] has been specified in the operand. This register can be used for loading LCD segment decoding operations, radio band edge data and the data related to binary to BCD conversion.

The DAL address register (DA) is 14-bit register for which specified the program memory indirectly when the DAL instruction is executed. There are two kinds of operation methods of DAL instruction. The control is selected by DAL bit. When DAL bit is set "0", ADDR3 (6 bits) of the operand and contents of general register (r) becomes the reference address of program memory and when DAL bit is set "1", 14 bit of DAL address register becomes reference address. At the time of setting DAL bit is "0" and execution of DAL instruction, only program memory area (0000H~03FF) becomes reference area and DAL bit is set "1" and execution of DAL instruction, all program memory area (0000H~3FFFH) becomes reference area.

If (DATA) → DA bit is set to "1", it can transfer from the contents of data register to 14-bit DAL address register by executing of single instruction.

The contents of DAL address register are accessed the data in 4-bit units with the execution of the OUT3/IN3 instruction for which [CN = BH] have been specified in the operand. DAL address register port is setup by data select port (ϕL2D) for which divides and indirect specified. The data of a specification port to set beforehand is set and the data port corresponding to it is accessed. Data select port is +1 incremented whenever is accessed this port (ϕL3B, ϕK3B). For this reason, after setting up a data selection port, it can access continuously.

DAL bit and (DATA) → DA bit are accessed with the execution of OUT3/IN3 instruction for which [CN = AH] has been specified in the operand.

Note: DAL address register becomes effective only execution of DAL instruction when setting "1" and becomes unrelated at the time of other instruction execution. It does not have the influence on this register by DAL instruction.

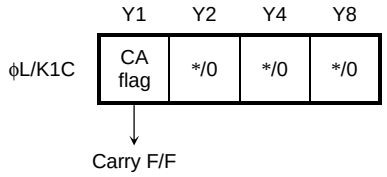
Note: For this product have 8 K step of ROM Capacity, If 2000H - 3FFFH is specified to be DAL address register and DAL instruction is executed, the contents of a data register will become unfixed.

Note: It's possible to write in and read out for data registeter and DAL address register. Please evacuate and return in a data memory if needed at the time of interruption.

Note: There is no action when (DATA) → DA bit is set "0". When it accesses to ϕK3A, it only read out only the DAL bit. (The other bit is "0".)

3. Carry F/F (Ca flag, ϕKL1C)

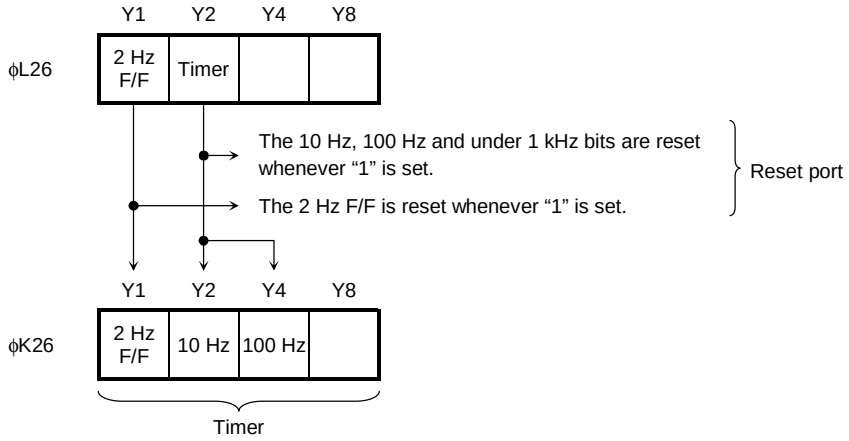
This is set when Carry or Borrow is issued in the result of calculation instruction execution and is reset if neither of these is issued. The carry F/F is accessed with OUT1/IN1 instructions for which [CN = CH] have been specified. For this reason, evacuation and a return of the carry F/F at the time of interruption can be performed easily. Carry F/F is written in a data memory by IN1 instruction at the time of evacuation, it is evacuated, and the data evacuated by OUT1 instruction is transmitted to carry F/F from a data memory after the time of a return.



○ Timer Port

The timer is equipped with 100-Hz, 10-Hz and 2-Hz F/F bits and used for counting clock operations and tuning scan mode, etc.

1. Timer Port

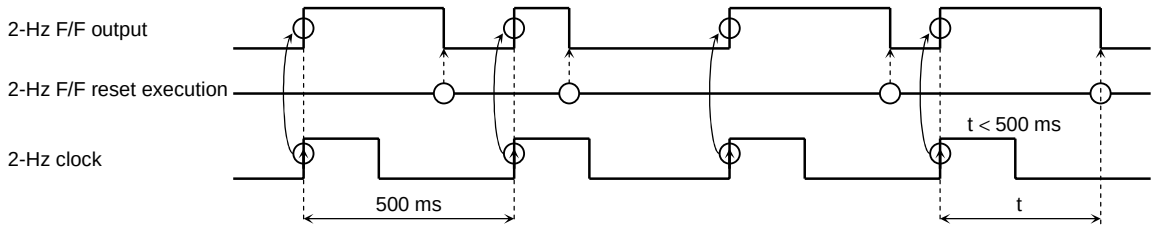


The timer ports are accessed with the OUT2/IN2 instructions for which [CN = 6H] has been specified in the operand

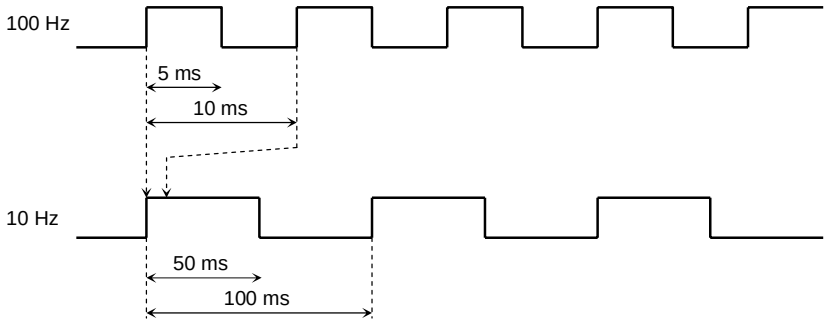
2. Timer Port Timing

The 2-Hz timer F/F is set with the 2-Hz (500 ms) signal and is reset by setting "1" in the reset port's 2-Hz F/F. This bit is usually used as a clock counter.

The 2-Hz timer F/F can only by reset with the reset port's 2 Hz F/F, and incorrect counts will be output and correct timers not acquired if not reset within a 500 ms cycle.



The 10-Hz and 100-Hz timers are outputted to 10-Hz and 100-Hz bits with a duty 50% of 100-ms and 10-ms cycles respectively. Counters at 1 kHz or below will be reset whenever the reset port's timer bit is set at "1".



○ Output Port (Used as LCD Driver Pin)

There are 18-output ports of CMOS type. These output port are used as LCD driver and changed output port by V_{LCD} OFF bit. If V_{LCD} OFF bit is set to "1", this port becomes output port. The outputted data to output port is used as segment data port-1 (ϕL2E). This data is accessed with OUT2 instruction for which [CN = EH] is specified and is setup by data select port (ϕL2D) for which divides and indirect specified like segment data. The data of a specification port to set a segment data port is set beforehand, and the data port corresponding to it is accessed. The data select port is +1 incremented whenever it accesses segment data port-1 (ϕL2E). For this reason, after setting up a data selection port, it can set up continuously.

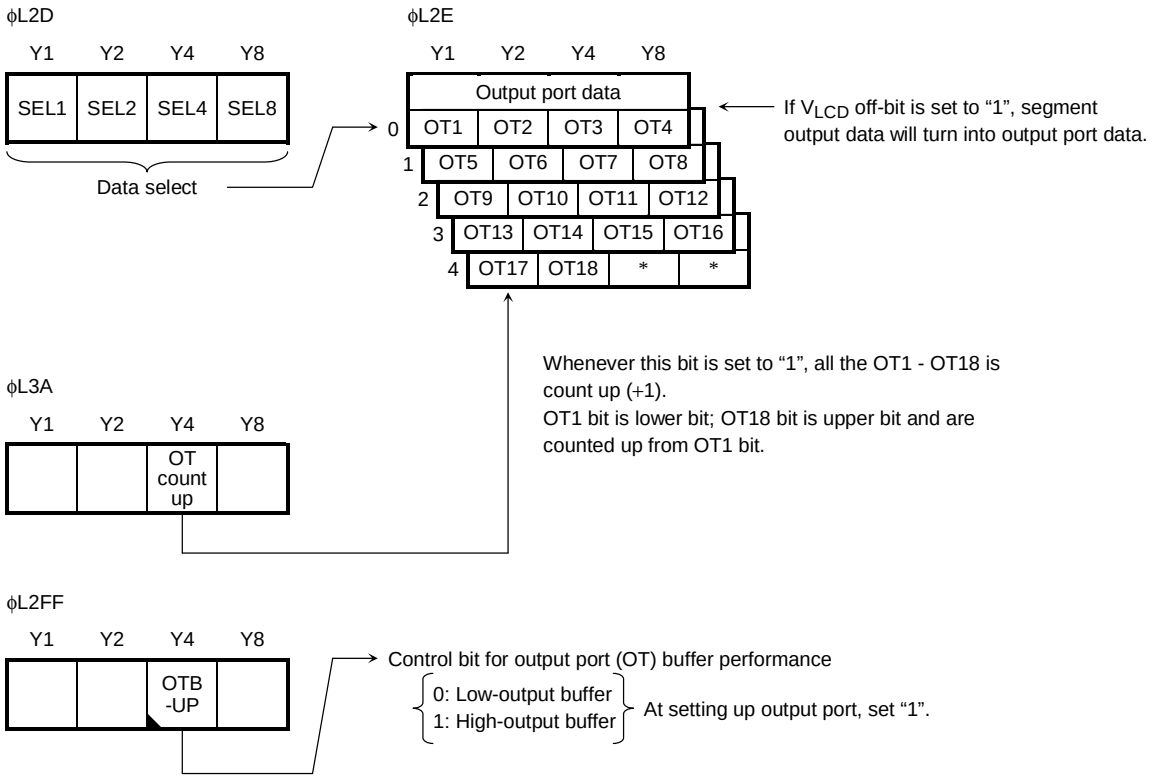
Output data is +1 increment with OT count UP bit by executing one instruction. For this reason, it can use as an address signal output when using an external memory etc. Output buffer capability can be changed at the time of an output setup. If OTB-UP bit is set "0", it becomes low output buffer (same performance of LCD output driver) and set "1", it becomes high output buffer. Usually, at the time of an output port setup, this bit is set to "1".

The power supply of this output port is used V_{LCD} dobuler potential, when using it as an output port, remove for the capacitor of V_{LCD} doubler potential (between C3-C4) and connect V_{LCD} pin with V_{DD} pin.

Note: Data select port is +1 increment automatically whenever it accesses ϕL2E, ϕL2F, ϕL3B, ϕK3B on I/O map.

Note: If set "0" to OT count UP bit, it does not perform count-up.

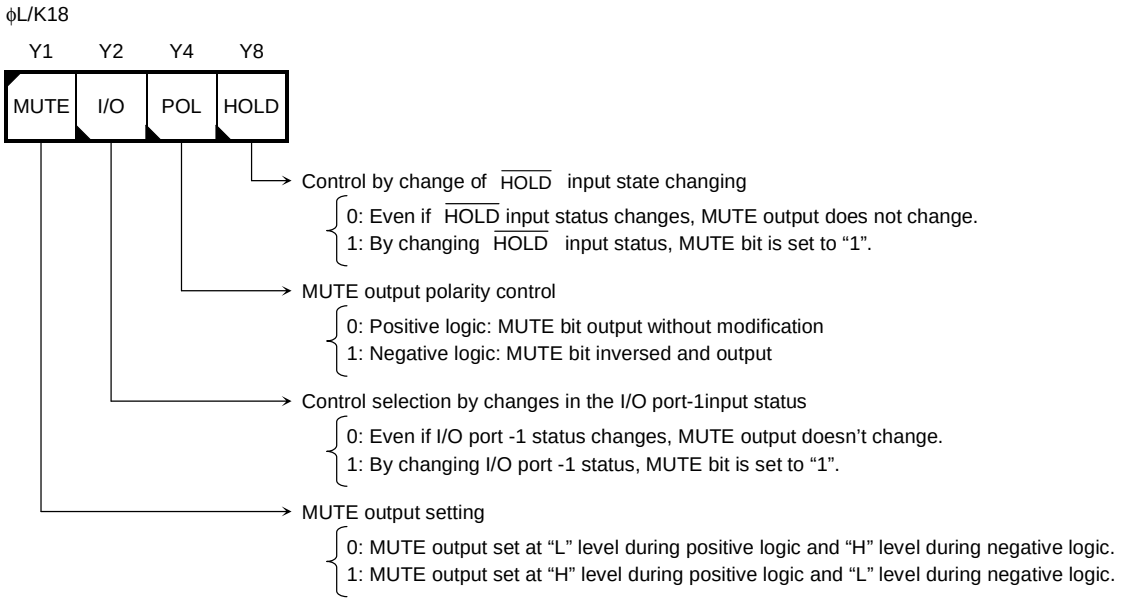
Note: Refer to LCD driver item.



○ MUTE Output

This is a 1-bit CMOS output port for muting control purposes.

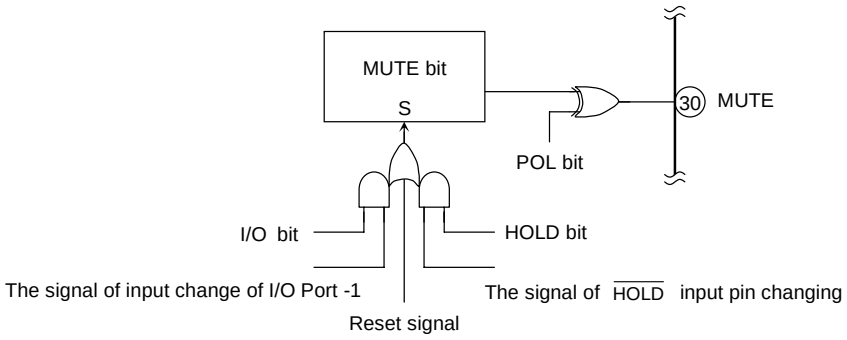
1. MUTE Port



This port is accessed with the OUT1/IN1 instruction for which [CN = 8H] has been specified in the operand. MUTE output is used for muting control. Setting the MUTE bit to "1" suppresses the generation of noise when the linear circuit is switched, for example when the equipment is powered down, or when the I/O Port 1 input or $\overline{\text{HOLD}}$ input is used to switch band. This control is set up according to the contents of I/O bit and HOLD bit. POL bit sets up the logic of MUTE output.

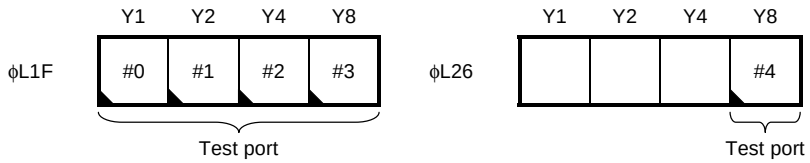
Please set up according to specification.

2. Circuit Configuration of MUTE Output



○ Test Port

This internal port is to test device function. It is accessed with OUT1 instruction specifying [CN = FH] and OUT2 instruction specifying [CN = 6H] in the operand.



○ Application to an Emulator Tip

If TEST pin is supplied “H” level (Test mode), the device operates as an emulator chip. Three kinds of test modes are prepared and can constitute a soft development tool by using three devices.

Radio operation can be checked by the connection between this soft development tool and IC for tuners, performing soft development.

Please refer to TC9328FA software development tool specifications of a development tool.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~4.0	V
Voltage doubler boosting voltage	V_{DB}	−0.3~4.0	V
Output voltage 1 (N-channel open drain)	V_{O1} (*)	−0.3~4.0	V
Output voltage 2 (N-channel open drain)	V_{O2} (*)	−0.3~V_{DB} + 0.3	V
Output voltage 3 (N-channel open drain)	V_{O3} (*)	−0.3~V_{LCD} + 0.3	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	100	mW
Operating temperature	T_{opr}	−10~60	°C
Storage temperature	T_{stg}	−65~150	°C

*: V_{O1}: P3-0~P3-3, P6-0~P6-3, P7-0~P7-3 pin
V_{O2}: P5-0~P5-3 pin
V_{O3}: P8-0~P8-3, P9-0~P9-3 pin

Electrical Characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 1.8 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Range of operating supply voltage	V_{DD1}	—	Under CPU operation (*)	0.9	~	1.8	V
	V_{DD2}	—	Under PLL operation (*)	0.9	~	1.8	
Range of memory retention voltage	V_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed) (*)	0.75	~	1.8	V
Operating current	I_{DD1}	—	PLL operation (VHF mode) at input FMin = 230 MHz	—	6	10	mA
	I_{DD2}	—	Under CPU operation only (PLL off, display turned on)	—	40	80	μA
	I_{DD3}	—	Hard wait mode (crystal oscillator operating only)	—	20	40	
	I_{DD4}	—	Soft wait mode (CPU stopped, PLL off)	—	30	—	
Memory retention current	I_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed)	—	0.1	1.0	μA
Crystal oscillation frequency	f_{XT}	—	(*)	—	75	—	kHz
Crystal oscillation start-up time	t_{st}	—	Crystal oscillation f_{XT} = 75 kHz	—	—	1.0	s

For conditions marked by an asterisk (*), guaranteed when V_{DD} = 0.9~1.8 V, Ta = −10~60°C

Voltage Doubler Boosting Circuit

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Doubled voltage	V_{DB}	—	GND reference (V_{DB})	—	$V_{DD} \times 2$	—	V
Doubled voltage output current	I_{DB}	—	$V_{OH} = V_{DB} - 0.1$ V (V_{DB})	–50	–200	—	μA
Doubled voltage reference voltage	V_{EE}	—	GND reference (V_{EE})	1.35	1.50	1.65	V
Constant voltage for phase comparator	V_{reg}	—	GND reference (V_{reg})	1.35	1.50	1.65	V
Constant voltage temperature characteristic	Dv	—	GND reference (V_{DD}, V_{reg})	—	–5	—	mV/°C
Power supply output current for phase comparator	I_{reg}	—	$V_{OH} = V_{reg} - 0.1$ V (V_{reg}) (Note 1)	–50	–200	—	μA
Doubled voltage	V_{LCD}	—	GND reference (V_{LCD})	2.7	3.0	3.3	V
Doubled voltage output current	I_{LCD}	—	$V_{OH} = V_{LCD} - 0.1$ V (V_{LCD}) (Note 1)	–50	–200	—	μA

Note 1: The “H” level output current of the pin using the V_{reg}/V_{LCD} power supply must not exceed the power supply (doubled voltage: V_{DB}) output current.

Programmable Counter/IF Counter Operating Frequency Range

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FMin (VHF mode)	f VHF	—	$V_{IN} = 0.1\ V_{p-p}$ (*)	50	~	230	MHz
FMin (FM mode)	f FM	—	$V_{IN} = 0.1\ V_{p-p}$ (*)	30	~	130	MHz
AMin (HF mode)	f HF1	—	$V_{IN} = 0.1\ V_{p-p}$ (*)	3.0	~	30	MHz
	f HF2	—	$V_{IN} = 0.1\ V_{p-p}$ (*)	1.0	~	10	
AMin (LF mode)	f LF	—	$V_{IN} = 0.1\ V_{p-p}$ (*)	0.5	~	8	MHz
IFin1, IFin2	f IF	—	$V_{IN} = 0.1\ V_{p-p}$ (*)	0.3	~	12	MHz
PSC transfer delay time	tpd	—	(PSC) $C_L = 15$ pF, $V_{DD} = 1.1$~1.8 V (*)	—	—	400	ns

*: Guaranteed when $V_{DD} = 0.9$~1.8 V, Ta = –10~60°C

Programmable Counter/IF Counter Input Amplitude Range

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FMin (VHF mode)	V VHF	—	Same as for f VHF (*)	0.1	~	0.6	V_{p-p}
FMin (FM mode)	V FM	—	Same as for f FM (*)	0.1	~	0.6	V_{p-p}
AMin (HF mode)	V HF	—	Same as for f HF1~2 (*)	0.1	~	0.6	V_{p-p}
AMin (LF mode)	V LF	—	Same as for f LF (*)	0.1	~	0.6	V_{p-p}
IFin1, IFin2	V IF	—	Same as for f IF (*)	0.1	~	0.6	V_{p-p}

*: Guaranteed when $V_{DD} = 0.9$~1.8 V, Ta = –10~60°C

LCD Common Output/Segment Output (COM1~COM4, S1~S22)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH1	—	V_{LCD} = 3 V, $V_{OH} = V_{LCD} - 0.3$ V (COM1~COM4)	–0.10	–0.20	—	mA
		IOH2	—	V_{LCD} = 3 V, $V_{OH} = V_{LCD} - 0.3$ V (S1~S22)	–0.05	–0.10	—	
	"L" level	IOL1	—	V_{LCD} = 3 V, V_{OL} = 0.3 V (COM1~COM4)	0.10	0.30	—	
		IOL2	—	V_{LCD} = 3 V, V_{OL} = 0.3 V (S1~S22)	0.05	0.15	—	
Output voltage 1/2 level		VBS	—	No load (COM1~COM4)	1.35	1.5	1.65	V

Output Port, I/O Port (OT1~OT18, P8-0~P8-3, P9-0~P9-3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH3	—	V_{LCD} = 3 V, $V_{OH} = V_{LCD} - 0.3$ V (Note 1, except I/O port)	–1.5	–3.0	—	mA
	"L" level	IOL3	—	V_{LCD} = 3 V, V_{OL} = 0.3 V	1.5	3.0	—	
Input leak current		ILI	—	$V_{IH} = V_{LCD}$, V_{IL} = 0 V (P8-0~P8-3, P9-0~P9-3)	—	—	±1.0	μA
Input voltage	"H" level	V_{IH}	—	(P8-0~P8-3, P9-0~P9-3)	$V_{DD} \times 0.8$	~	V_{DD}	V
	"L" level	V_{IL}	—	(P8-0~P8-3, P9-0~P9-3)	0	~	$V_{DD} \times 0.2$	

Note 1: The "H" level output current is the current when the pin power supply is fixed.
Make sure that pins using V_{reg}/V_{LCD} power supply do not exceed the power supply (doubled voltage: V_{DB}) output current.

I/O Port (P1-0~P7-3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH4	—	V_{DD} = 1.5 V, V_{OH} = V_{DD} − 0.2 V (I/O port P2, P4)	−0.4	−0.8	—	mA
		IOH5	—	V_{DD} = 0.9 V, V_{OH} = V_{DD} − 0.2 V (I/O port P2, P4)	−0.04	−0.2	—	
	"L" level	IOL4	—	V_{DD} = 1.5 V, V_{OL} = 0.2 V (except I/O port P3)	0.5	1.0	—	
		IOL5	—	V_{DD} = 0.9 V, V_{OL} = 0.2 V (except I/O port P3)	0.1	0.3	—	
		IOL6	—	V_{DD} = 0.9~1.8 V, V_{OL} = 0.2 V (I/O port P3)	1.0	2.0	—	
Input leak current		ILI	—	V_{IH} = V_{DD}, V_{IL} = 0 V (I/O port P1, P2, P4)	—	—	±1.0	μA
			—	V_{IH} = 3.6 V, V_{IL} = 0 V (I/O port P3, P6, P7)	—	—	±1.0	
			—	V_{IH} = V_{DB}, V_{IL} = 0 V (I/O port P5)	—	—	±1.0	
Input voltage	"H" level	V_{IH}	—	—	V_{DD} × 0.8	~	V_{DD}	V
	"L" level	V_{IL}	—	—	0	~	V_{DD} × 0.2	
Input pull-down resistor		RIN1	—	When P1-0~P1-3 are set to pull-down or pull-up	30	60	120	kΩ
SCK clock external input frequency		f_{SIO}	—	When I/O port P4-3 are set to serial clock input	—	—	200	kHz

For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8~3.6 V, Ta = −10~60°C

Note 1: The "H" level output current is the current when the pin power supply is fixed.
Make sure that pins using V_{reg}/V_{LCD} power supply do not exceed the power supply (doubled voltage: V_{DB}) output current.

MUTE Output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH4	—	V_{DD} = 1.5 V, V_{OH} = V_{DD} − 0.2 V	−0.4	−0.8	—	mA
		IOH5	—	V_{DD} = 0.9 V, V_{OH} = V_{DD} − 0.2 V	−0.04	−0.2	—	
	"L" level	IOL4	—	V_{DD} = 1.5 V, V_{OL} = 0.2 V	0.5	1.0	—	
		IOL5	—	V_{DD} = 0.9 V, V_{OL} = 0.2 V	0.1	0.3	—	

$\overline{\text{HOLD}}$, INTR1/2, IN1/2 Input Port, $\overline{\text{RESET}}$ Input

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leak current		ILI	—	V_{IH} = V_{DD}, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH3}	—	—	VDD × 0.8	~	V_{DD}	V
	"L" level	V_{IL3}	—	—	0	~	V_{DD} × 0.2	

AD Converter (ADin1~ADin4)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog input voltage range	VAD	—	ADin1~ADin4	0	~	V_{DB}	V
Resolution	VRES	—	—	—	6	—	bit
Conversion total error	—	—	—	—	±0.5	±1.0	LSB
Analog input leak	ILI	—	$V_{DD} = V_{DB}$, $V_{IH} = V_{DB}$, $V_{IL} = 0$ V (ADin1~ADin4)	—	—	±1.0	μA

DO1, DO2 Output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH4	—	V_{reg} = 1.5 V, $V_{OH} = V_{reg} - 0.2$ V (Note 1)	–0.4	–0.8	—	mA
	"L" level	IOL4	—	V_{reg} = 1.5 V, V_{OL} = 0.2 V	0.5	1.0	—	
Output off leak current		ITL	—	V_{DD} = 1.5 V, V_{TLH} = 1.5 V, V_{TLL} = 0 V	—	—	±100	nA

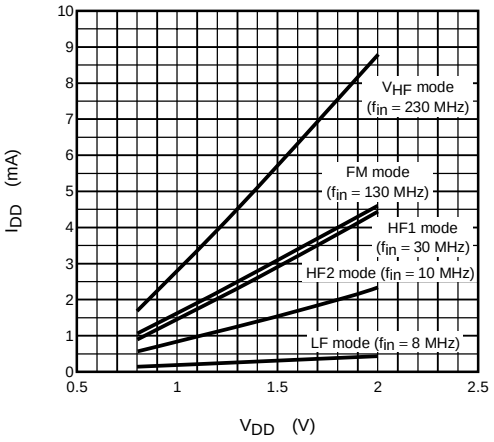
Others

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input pull-down resistance	RIN2	—	(TEST)	5	10	30	kΩ
XIN amp. feedback resistance	RfXT	—	(XIN-XOUT)	—	20	—	MΩ
XOUT output resistance	ROUT	—	(XOUT)	—	4	—	kΩ
Input amp. feedback resistance	Rf_{IN1}	—	(FMin)	100	200	400	kΩ
	Rf_{IN2}	—	(AMin, IFin1, IFin2)	300	600	1200	

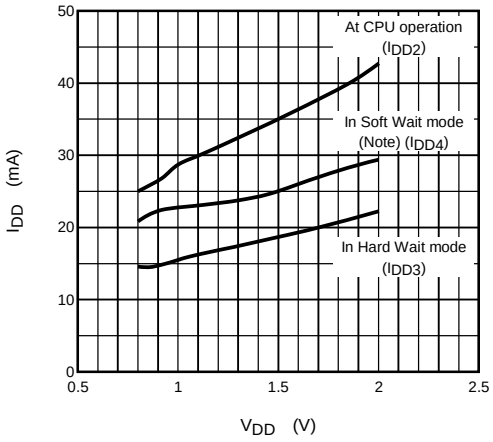
For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8~3.6 V, Ta = –10~60°C

Note 1: The "H" level output current is the current when the pin power supply is fixed.
Make sure that pins using V_{reg}/V_{LCD} power supply do not exceed the power supply (doubled voltage: V_{DB}) output current.

Typical TC9328AF product
I_{DD} (Ta = 25°C) in different modes at PLL operation

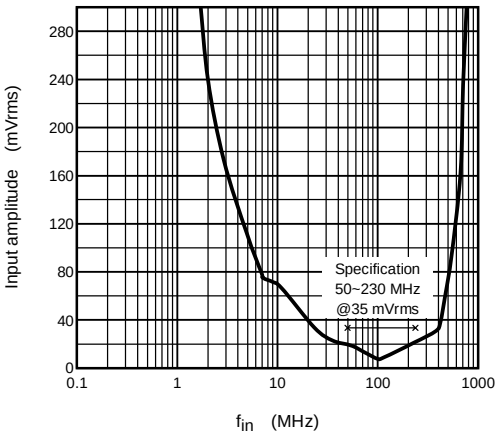


Typical TC9328AF product
I_{DD} (Ta = 25°C) in different modes at CPU operation

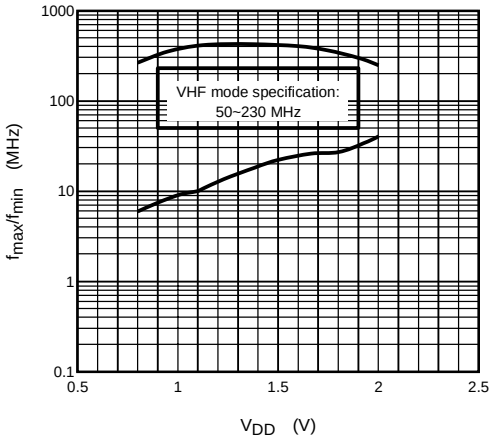


Note: The I_{DD} (operating current) in Soft Wait mode is the current dissipation value.
The actual current dissipation value differs depending on the CPU execution state.

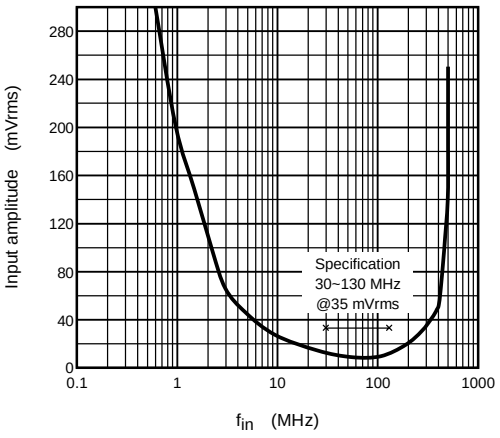
Typical TC9328AF product input sensitivity VHF mode
(V_{DD} = 1.5 V, Ta = 25°C)



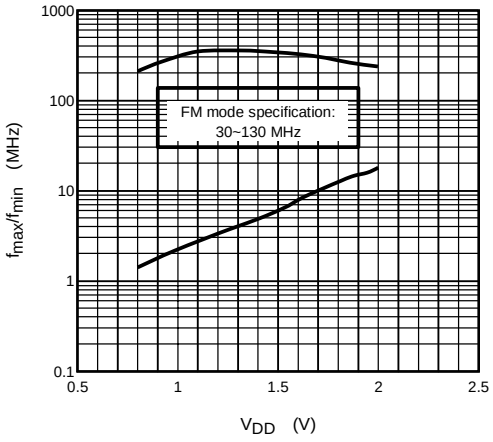
Typical TC9328AF product input sensitivity VHF mode
V_{DD} – f_{max}/f_{min} (V_{in} = 35 mVrms, Ta = 25°C)



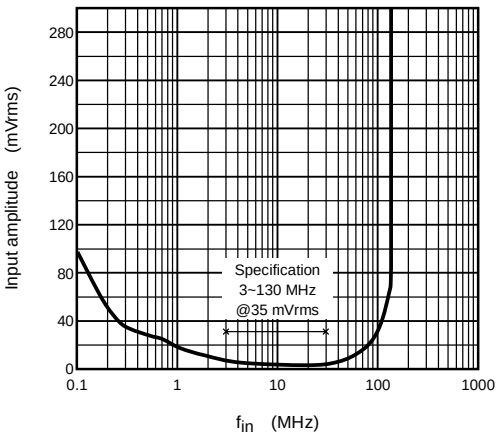
Typical TC9328AF product input sensitivity FM mode
(V_{DD} = 1.5 V, Ta = 25°C)



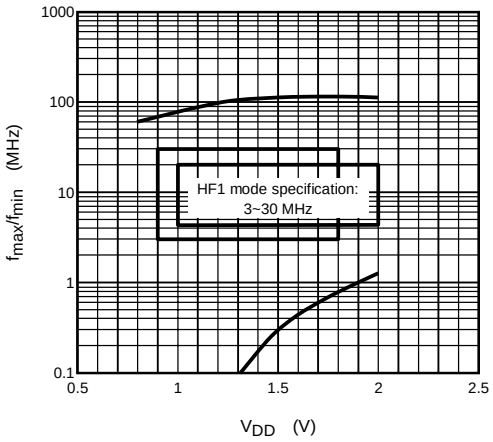
Typical TC9328AF product input sensitivity FM mode
V_{DD} – f_{max}/f_{min} (V_{in} = 35 mVrms, Ta = 25°C)



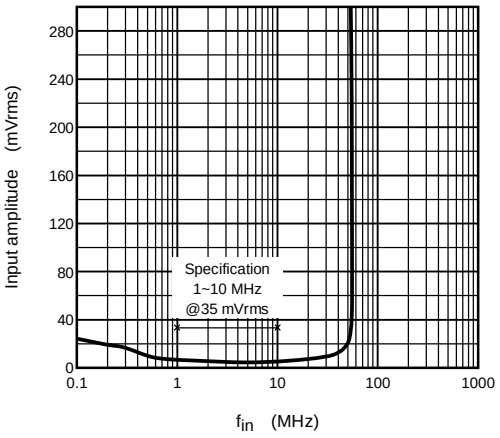
Typical TC9328AF product input sensitivity HF1 mode
(V_{DD} = 1.5 V, Ta = 25°C)



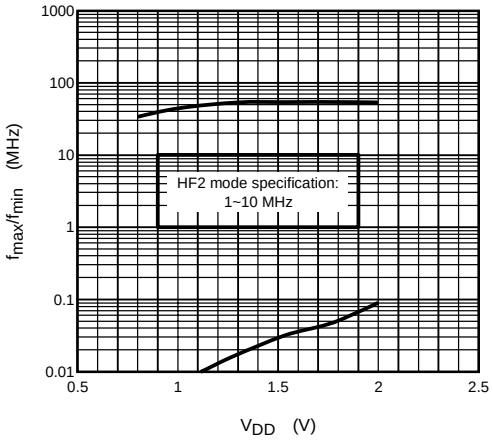
Typical TC9328AF product input sensitivity HF1 mode
V_{DD} – f_{max}/f_{min} (V_{in} = 35 mVrms, Ta = 25°C)



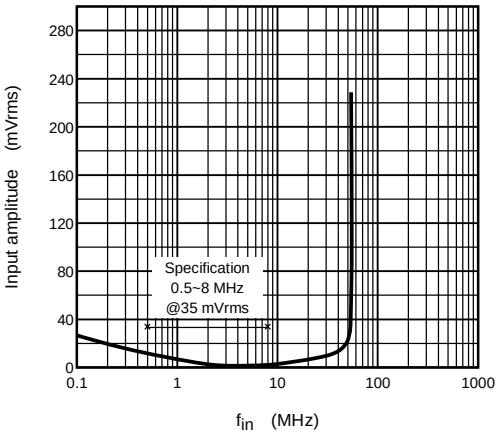
Typical TC9328AF product input sensitivity HF2 mode
(V_{DD} = 1.5 V, Ta = 25°C)



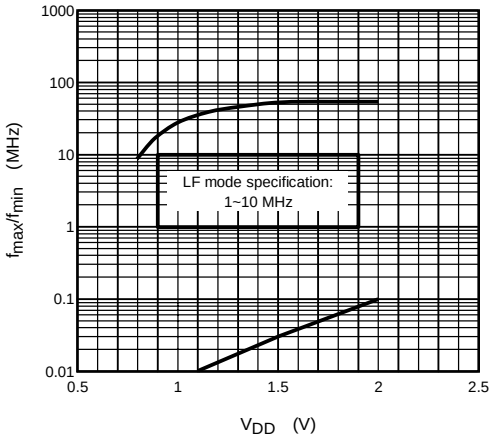
Typical TC9328AF product input sensitivity HF2 mode
V_{DD} – f_{max}/f_{min} (V_{in} = 35 mVrms, Ta = 25°C)



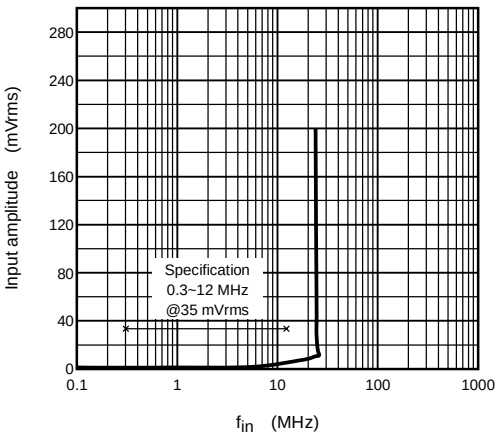
Typical TC9328AF product input sensitivity LF mode
(V_{DD} = 1.5 V, Ta = 25°C)



Typical TC9328AF product input sensitivity LF mode
V_{DD} – f_{max}/f_{min} (V_{in} = 35 mVrms, Ta = 25°C)

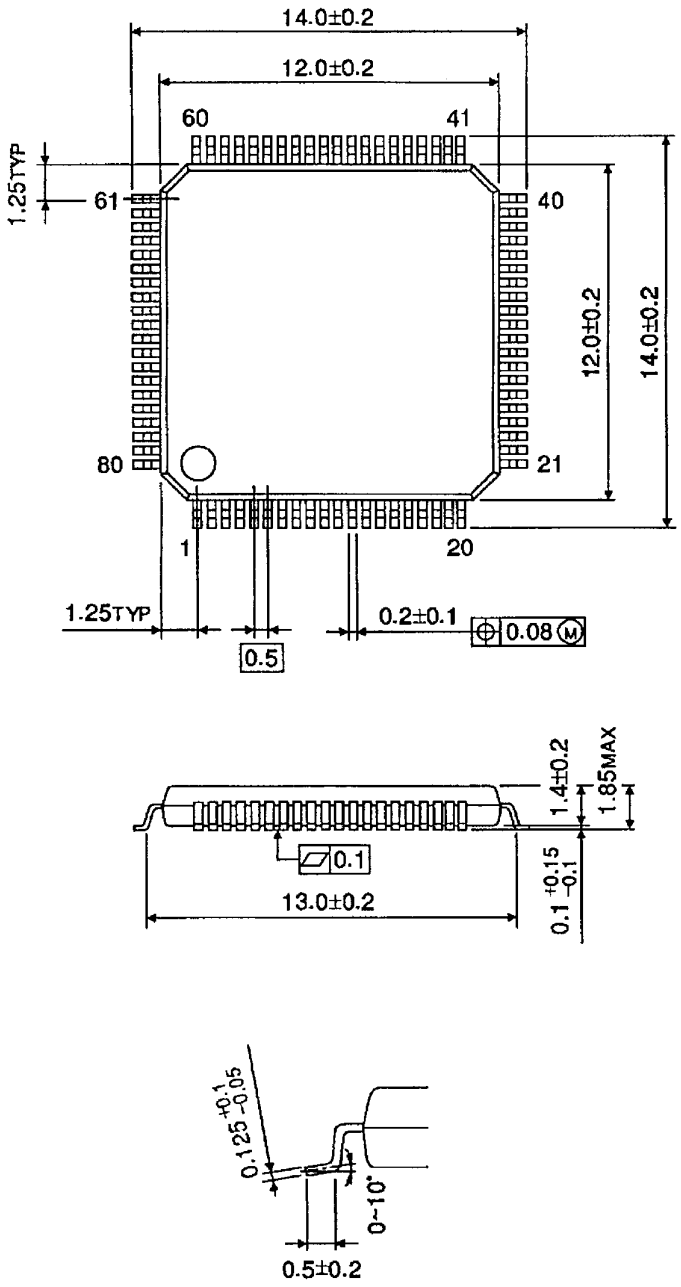


Typical TC9328AF product input sensitivity IFin mode
(V_{DD} = 1.5 V, Ta = 25°C)



Package Dimensions

LQFP80-P-1212-0.50A Unit : mm



Weight: 0.45 g (typ.)

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